[A-123]

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SARDAR PATEL UNIVERSITY

Post Graduate Diploma in Computer Applications (PGDCA)

Semester – I External Examinations

PGDCA-103 Logical Organization of Computers Monday, April 4th, 2016

Time: 02:30 p.m. to 05:30 p.m.				Max Marks: 70	
		most appropriate option fo	or each questi	on:	[8]
1.	A nibble is	a group of bits.			
	A.	4	В.	16	
2	C.	8	D.	32	
۷.	Full form of				
	A. C.	Central Processing Unit Computer Processing Unit	В. D .	Central Process Unit	
3.		$0)_2 = (\underline{}_{8}$	D.	Central Programming Unit	
	Α.	1063	В.	1064	
	C.	164	D.	None of these	
4.	In hexadec	imal number system, A is	equal to	decimal number	
	A.	10	B.	11	
_	C.	17	D.	18	
5.		ate is also called a			
	A. C.	NOT NAND	В. D.	XNOR	
6.		consist of & _		NOR .s	
	Α.	XOR, AND	В.	XOR, OR	
	C.	XNOR, AND		XNOR,OR	
7.	A combinat	tional circuit that performs	the arithmetic	c addition of three bits is called	
		hinan, adda.	D		
	A. C.	binary adder multiplexer	В. D.	decoder Full Adder	
8.	8. De Morgan's first theorem says that a NOR gate is equivalent to a				
	Α.	bubbled OR	В.	bubbled NOR	•
	C.	bubbled AND	D.	AND bubbled	
Q-2	Answer the	following questions (Any S	Seven):		[14]
1.	List the ste	ps of Fetch decode execu	te cycle.		
		lock diagram of a simple of	computer.		
	Define: Inte	•		•	
		truction Register?			
	Describe th				
	Define: Bin	it diagram for A B C+ B C			
/•	Denne. Din	ary Adder.			

8	3. Define Logic Circuit and Boolean Algebra		
). What is a Parity bit?		
Q-3	Answer the following questions:		
A.	. Discuss Pipelining for Instruction-Level Parallelism.	16	
	Explain sign magnitude method for integer representation.	[6	
	OR	[6	
В.	. Write a note on different types of instructions.	[6	
		Į0	
Q-4	Answer the following questions:		
A.	Explain IEEE Floating Point representation.	[6	
	. Write a note on the working of laser printers.	[6	
	OR	Į	
В.	Discuss the designing criteria for Instruction Formats.	. [6	
Q-5	Answer the following questions:		
	Explain AND, NOR, XOR gate with truth tables.	16	
В.	Explain half adder in detail.	[6]	
	OR	[6]	
В.	What is demultiplexer? Explain 1 to 8 demultiplexer in detail		
	explain 1 to 0 demaniplexer in detail	[6]	
Q-6	Answer the following questions:		
A.	Write a note on shift Right register in detail.		
В.	Explain Ring counter.	[6]	
	OR	[6]	
В.	Discuss Clocked and Unclocked D Flip-Flop.		
	The state of the s	[6]	