No. of Printed Pages: 02

[80-A]

SARDAR PATEL UNIVERSITY

M.Sc. (Semester III) (CBCS) EXAMINATION 2012

Friday, 7th December 2012

P S 0 3 E E L C 0 1

CMOS Technology & VLSI Design

Time: 02:30 PM TO 05:30 PM

| | | | | | | Total Marks: 70 | | | |
|-------|------|--|---|------------------------------|------------|---------------------------------------|------------|--|--|
| Q - 1 | Mult | iple Cho | pice Question | | | | [8] | | |
| | 1. | Whic | h Statement is true fo | or Stati | c RAM. | | | | |
| \$96 | | i) Single ended output ii) Slower so used for main memory iii) Data is stored as long as supply is applied iv) None of above | | | | | | | |
| | 2. | The Moore machine o/p is depend on | | | | | | | |
| | | i) iii) | Current state, I/p Current state, Next | state | ii) iv) | Next state Current state | | | |
| 11 | 3. | What Does Stand For UART | | | | | | | |
| | 15.1 | Universal Asynchronous Receive Transmit Universal Asynchronous Receiver Transmit Universal Asynchronous Receiver Transmitter Universal Asynchronous Receiver Transmitton. | | | | | 13 | | |
| | 4. | What does stand for DDR SDRAM? | | | | | | | |
| | | i) ii) iii) iv) | Dual data rate SDRA Dual double rate SD Double dual rate SD Double data rate SD | RAM. RAM. | | | | | |
| | 5. | In CPLD XC9572 series what does mean of 4/72 | | | | | | | |
| | | i) iii) | Macro cells / FBs Macro cells / Output | pin | ii) iv) | FBs / Input pin FBs / Macro cells | Berger St. | | |
| | 6. | What Does mean of DUT ? | | | | | | | |
| | | i) iii) | Data Under Test Design Under Test | ii) iv) | | n Upper Test e True | 22 | | |
| | 7. | Which | statement is true? | | | | | | |
| | | i) iii) | Ieee.std_logic_1164 leee.std_logic_1164 | _all | II) iv) | IEEE_STD_LOGIC_1164 A None of all. | | | |
| | 8. | A Transmission Gate is a combination ofand also known as | | | | | | | |
| | | i) ii) iii) iv) | ii) Parallel PMOS and NMOS, Pass gate. iii) Parallel MOSFET AND CMOS, Basic gate | | | | | | |
| Q -2 | Answ | Answer the Following Questions (Any seven). | | | | | | | |
| | | 1) Write Down the VHDL Code for AND gate & NAND gate. 2) Write Down the Comparison of SRAM and Antifuse FPGA. 3) Write Down the CMOS Parasitic equivalent circuit. 4) Give The Description Of SRC And DRC. | | | | | | | |
| | | 6) Wri 7) Def 8) Wri | ine Body effect with one of the down the Definition in Why to prefer FPG te Down the Types Of the Transmission Gate | n of FSI iA's? Attribu | M with | Mealy circuit diagram. | 2.28 | | |

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| | 33 | 100 | Q -3 | Answer the Fo | ollowing Questions. | | |
|----|----|-------|--------|-------------------|--|--|-------|
| | | | | | e down the Architecture of FPGA wi | th diagram. | [6] |
| 2 | | 411 | М. | 7. | ain the Configuration in detail. | | [6] |
| 20 | | W. H | | b) Descr two o | ribe memory basics with types of m of Following in short details. 1) RA | nemory and define any M 2) ROM 3) Flash Memor | y [6] |
| | 14 | | Q -4 | Answer the Foll | lowing Questions. | | |
| | 72 | 5 35 | | a) Descr | ribe FSM in Detail with circuit diagra | am. | [6] |
| | | | | b) Expla | in the TEST BENCHES in detail. | 14 | [6] |
| | 9 | | | b) Explai | in The SRAM and DRAM Operation. | 78 | [6] |
| | | | Q -5 | Answer the Follo | owing Questions. | | |
| | | ě | 3 | a) Write | down the Architecture of CPLD with | h diagram. | [6] |
| | | 800 | | b) Descri | ibe Different modeling styles with o | one example. | [6] |
| | | | | b) Draw (| OR the VLSI Design Flow with Descript | ion. | [6] |
| | | | Q -6 / | Inswer the Follo | owing Questions. | | |
| | | | | a) Write | Down Programming of TLC. | | [6] |
| | | W. 51 | | b) Define | the Clock distribution and Power d | istribution in detail. | [6] |
| | | | | b) Descrit | be Global routing, Switch box routing | ng and Wire parasitic. | [6] |

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