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SARDAR PATEL UNIVERSITY
M.Sc. (Semester I) (CBCS) EXAMINATION 2016
(EC)
28th October 2016

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Computer Architecture and Organization

Time: 10:00 AM TO 1:00 PM
Total Marks: 70

Q-1 **Choose the correct answer.** **[08]**

1 Which of the following is exact symbolic representation of STA instruction?
   a) M[AR]←PC, PC←AR+1
   b) PC←AR
   c) M[AR]←AC
   d) AC←AR

2 Which instruction execution occurs for the condition $D_7I'T_3B_7$?
   a) CMA b) CME c) CIR d) SZE

3 Which is not a 16 – bit register?
   a) DR b) AC c) PC d) TR

4 If *h* is no. of hits and *m* is no. of misses, then hit ratio is defined as _____.
   a) *h/(h+m)* b) *m/(h - m)* c) *m/(h+m)* d) *h/(h - m)*

5 How many steps would be required to calculate following expression using RPN in stack operation?
   A*B+C*D+E*F
   a) 9 b) 10 c) 11 d) 12

6 Memory that uses the property of locality of reference is _____.
   a) Associative Memory b) Cache Memory
   c) Auxiliary Memory d) Main Memory

7 If IR contains 1111100000000000, what is the type of instruction?
   a) Indirect Memory Reference Instruction.
   b) Direct Memory Reference Instruction.
   c) Register Reference Instruction.
   d) I/O Instruction.

8 Which instruction is initiated for decoder output D_0?
   a) AND b) LDA c) BSA d) ISZ

Q-2 Answer in short. **[ANY SEVEN]**. **[14]**

1 Explain BUN instruction
2 Draw the register configuration for decimal division and multiplication operation.
3 Convert following arithmetic notation from reverse Polish notation to infix notation.
   ABC * / D – EF/ *
4 Give the full form of UART and LRU
5 Define: Associative memory
6 Define: Semaphore
7 Convert the following arithmetic notation from infix notation to reverse Polish notation.
   $A + B - C * (D + E)$
8 Give Flynn's classification.
9 Explain FIFO

P.T.O.

Q-3	A	Draw common bus system	**[06]**
Q-3	B	Explain I/O instructions.	**[06]**
		OR	
Q-3	B	Explain conditional branch instructions.	**[06]**
Q-4	A	Explain program interrupt.	**[06]**
Q-4	B	Give characteristics of RISC and CISC.	**[06]**
		OR	
Q-4	B	Explain memory stack organization.	**[06]**
Q-5	A	Write a brief note on cache memory.	**[06]**
Q-5	B	Draw a flow chart on ADD and SUBTRACT operation.	**[06]**
		OR	
Q-5	B	Draw a flow chart on MULTIPLICATION operation.	**[06]**
Q-6	A	What do you mean by polling? Explain daisy chaining priority.	**[06]**
Q-6	B	Write a note on DMA.	**[06]**
		OR	
Q-6	B	Explain Memory Interleaving.	**[06]**

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