[197] SEAT No. _____ No. of Printed Pages : 3 SC

SARDAR PATEL UNIVERSITY
M.Sc.(ELECTRONICS) IV SEMESTER EXAMINATION
SUBJECT CODE: **PS04EELE21** PAPER : **Design of VLSI Systems**
DATE : 26-03-2019, TUESDAY TIME : 02.00 pm to 05.00 pm
TOTAL MARKS : 70

Q-1 Multiple choice questions. [08]

1 In VHDL, std_logic_1164 is a

(a) Data Type (b) Design Unit

(c) Library (d) Package

2 Which symbol is used for variable assignment?

(a) := (b) ==

(c) = (d) <=

3 What cannot be defined inside the process?

(a) variable (b) signal

(c) constant (d) none of the above

4 A VHDL design technique that connects prepackaged components using internal signals is known as.

(a) Structural Design (b) Data-flow Design

(c) Behavioral Design (d) Block Design

5 A *flip-flop* is an example of _____ type of electronic circuit.

(a) Sequential (b) Combinational

(c) Moore machine (d) Analog

6 In VHDL, *architecture* , is a

(a) Design Unit (b) Package

(c) Library (d) Data Type

7 Among the VHDL features, which language statements are executed at the same time in parallel flow?

(a) sequential (b) concurrent

(c) net-list (d) Test Bench

8 Which region is required to build p-MOS?

(a) P-substrate (b) Polysilicon

(c) n-well (d) p+

(P.T.O.)

Q-2 Short question. (Answer any **SEVEN**) [14]

1 Discuss the subtypes with examples as are used in VHDL.

2 What is multi valued logic? Describe briefly.

3 What is the difference between std_logic and std_logic_vector VHDL?

4 What do you mean by Synthesis?

5 Describe the salient features of VHDL language.

6 What Is The Purpose Of Design Rule Check (DRC)?

7 What is the difference between STD_LOGIC and BIT types?

8 Difference Between FPGA And CPLD?

9 Why are p-mos larger than n-mos in CMOS design?

Q-3 [a] Write a short note on structural style of modeling in VHDL with suitable example. [06]

[b] List and explain various types of delays In VHDL. [06]

OR

[b] Design a n-MOS on Si-Substrate. Represent the design using a layout considering various design rules. [06]

Q-4 [a] List and discuss the various Hardware modeling issues for HDL. [06]

[b] Write a VHDL code for 4 bit binary to BCD converter circuit. [06]

OR

[b] Write a VHDL code for 8 bit full adder circuit. [06]

Q-5 [a] Write a behavioral VHDL description for a 4-to-1 multiplexer. Model the multiplexer as a process block. [06]

[b] Explain the architecture of simple microcomputer ALU system using VHDL language. [06]

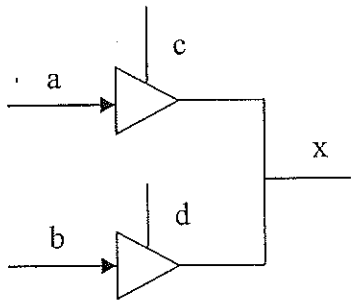
OR

[b] Discuss at length, the need and issues involved in Power and Ground line distributions in VLSI design? How are they solved? [06]

(2)

Q-6 [a] What is the Mealy machine's state diagram? Design a Mealy state diagram to detect 3 consecutive heads or tails of tossing of a coin. (Consider Resetting case) [06]

[b] Write a VHDL code for following tri-state buffer having active high output enable.



OR

[b] What do you mean by Reconfigurable Hardware? List and discuss about various technologies available in this domain of VLSI. [06]

— X —

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