SEAT No._____ No. of Printed Pages : 2

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SARDAR PATEL UNIVERSITY
M.Sc. (Electronics) I Semester Examination
Friday, 26th October, 2018 Time 10.00 am to 01.00 pm
PS01CELE23 - Microprocessor and Microcontroller Systems
Total Marks – 70

1. Figure to the right indicate maximum marks for the question

Q-1 **[08]**

A) In microprocessor the address of the new instruction to be executed is stored in _____.
i. Stack Pointer ii. PSW
iii. Program Counter iv. Memory

B) To differentiate Memory Mapped I/O and I/O Mapped I/O, which control pin of 8085 is used?
i. RD ii. ALE
iii. IO/M iv. None of the above

C) To interface 32 K of RAM memory, how many numbers of address lines are required?
i. 15 ii. 14
iii. 11 iv. 12

D) The control word value to configure 8155 for following is : Port A as Input, Port B and C as output.
i. 0E ii. 0C
iii.0F iv. 0D

E) 8155 has total _____ ROM locations of memory on it
i. 128 ii. 256
Iii. 2 K iv. none of the above

F) In 8255 PPI, Mode -1 is possible for followings:
i. Port A only ii. Port B only
iii. Port A and B iv. Port A, B and C

G) For 8051 Microcontroller, which of the following register can only be addressed as a byte?
i. P1 ii. SCON
iii. TMOD iv. TCON

H) For 8051, among the four groups of register banks, the number of groups that can be accessed at a time is
i. 1 ii. 2
iii. 3 iv. 4

Q-2 Answer any **seven**, in short.(Two marks each) **[14]**

1 What is linear addressing scheme in 8085 interfacing?
2 Design a circuit to obtain various control signals for interfacing in 8085 microprocessor based design.
3 With necessary timing diagram, explain the Handshake data Input process.

(PTO)

4 What is programmable peripheral device?
5 What is the function of PSEN pin of 8051?
6 Draw the Port-0 circuit of 8051 Microcontroller.
7 Is the number of output ports, in peripheral i/o, restricted to 256? Justify your answer.
8 Discuss, briefly, Stack mechanism in 8051.
9 Differentiate between Memory Mapped I/O and Peripheral I/O.

Q-3 [a] For following instructions, draw and explain the instruction execution timing diagram in detail: **[06]**

Address	Instruction
C000H	OUT
C001H	40H

Q-3 [b] Design the interface to use various ports of 8155. The addresses should start at address F0H. (Make necessary assumptions) **[06]**

OR

Q-3 [b] Design a circuit, with necessary control signals and chip select logic, to interface the memory(EPROM) of 8355 chip for the address-range A000h to A7FFh. **[06]**

Q-4 [a] The following memory devices are to be interfaced with 8085. **[06]**
(i) 2K E^2PROM (ii) 4K RAM. The EPROM address should start from location address 0000h & RAM at the location C000H. Draw the complete interface diagram.

Q–4 [b] Explain the control word format of 8253 timer IC. List various operating modes of 8253 timer IC and explain any one in detail with necessary diagram. **[06]**

OR

Q–4 [b] Explain the BSR mode of 8255 in detail. **[06]**

Q-5 [a] List the various address ranges available for various JUMP and CALL instruction in 8051 microcontroller. Explain each, with necessary example, in detail. **[06]**

Q-5 [b] Draw and describe the internal memory model of 8051 microcontroller. **[06]**

OR

Q-5 [b] Design an interface for external 16K EPROM and 8K RAM with the microcontroller 8051. **[06]**

Q–6 [a] List various SFR's of 8051 microcontroller. Explain, in detail, SFR's used for timer section of 8051. **[06]**

Q–6 [b] Write an assembly code of 8051 to count number of 0's in the data stored on the location R0 of Register Bank-1. Store the result in register R1 of Bank -2. **[06]**

OR

Q- 6 [b] What do you understand by BIT addressing? Explain the BIT addressing features of 8051 in detail. **[06]**

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