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SARDAR PATEL UNIVERSITY

M.Sc. (Electronics) I Semester Examination

Wednesday, 5th December, 2012 Time 10.30 am to 01.30 pm

PS01CELE03 - Microprocessor and Microcontroller Systems

Total Marks – 70

1. Figure to the right indicate maximum marks for the question

Q-1 **[08]**

A) If a 8-bit data buffer IC is to be interfaced with 8085 processor in memory mapped I/O mode, which control signal is used to move the data?

i. $\overline{MEMW}$ ii. $\overline{MEMR}$

iii. $\overline{IOR}$ iv. $\overline{IOW}$

B) To differentiate Memory Mapped I/O and I/O Mapped I/O, which control pin of 8085 is used?

i. $\overline{RD}$ ii. $\overline{ALE}$

iii. $IO/\overline{M}$ iv. None of the above

C) To interface 16 K of RAM memory, how many numbers of address lines are required?

i. 13 ii. 14

iii. 15 iv. 12

D) The control word value to configure 8155 for following is : Port A as input, Port B as input and Port C as input.

i. 03 ii. 3C

iii.00 iv. 0B

E) 8155 timer has total _____ locations of RAM on it

i. 128 ii. 256

Iii. 2 K iv. none of the above

F) In 8255 PPI, Mode -2 is possible for followings:

i. Port A only ii. Port B only

iii. Port A and B iv. Port A, B and C

G) In serial communication, it is a connection between two terminals such that data may travel in both direction at a time, is known as,

i. Simplex ii. Half Simplex

iii. Duplex iv. Half Duplex

H) To write 1 bit data to SOD line of 8085, which instruction is used?

i. IN ii.STA .....

iii. SIM iv. RIM

Q-2 Answer any **seven**, in short.(Two marks each) **[14]**

1. What is linear addressing scheme of 8085 interfacing.
2. With the help of a schematic diagram, explain how the bus AD7 – AD0 is demultiplexed.
3. With necessary timing diagram, explain the Handshake data output process.

P.T.O

4 What is asynchronous data transfer scheme?
5 What do you mean by level trigger and edge trigger signal?
6 Draw a circuit to generate the various control signals for I/O operation of 8085.
7 What is vector location in microprocessor? Explain with suitable example.
8 Differentiate between Interrupt driven data I/O and Polling Method of data I/O.
9 Why address bus of 8085 processor is unidirectional?

Q-3 [a] For following instructions, draw and explain the instruction execution timing diagram in detail: **[06]**

Address	Instruction
2000H	IN
2001H	40H

Q-3 [b] Design the interface to access 256 bytes of RAM of 8155. The RAM address should start at address FF00H. Give the range of memory. **[06]**

OR

Q-3 [b] With neat sketch of block diagram, explain the principal of interfacing and output device to microprocessor. **[06]**

Q-4 [a] Write a program segment to get a data byte from port B of 8255 and add FFh to this data. Output the results to port A. Assume that 8255 is configured in memory mapped I/O. Make necessary assumptions. **[06]**

Q-4 [b] List and explain the various operating modes of 8253 timer IC. **[06]**

OR

Q-4 [b] Explain the BSR mode of 8255 in detail. **[06]**

Q-5 [a] Compare the Parallel and Serial I/O in microprocessor based system. **[06]**

Q-5 [b] Illustrate SIM and RIM instructions of 8085 microprocessor used for serial communication with suitable example.. **[06]**

OR

Q-5 [b] The following memory devices are to be interfaced to 8085. **[06]**
(i) 2K EPROM (ii) 2K RAM. The EPROM address should start from location address 0000h & RAM at the location F000H. Draw the complete interface diagram.

Q-6 [a] Draw and explain the internal memory organization of 8051 micro-controller. **[06]**

Q-6 [b] How many timers are available in 8051 microcontroller?What are the SFRs associated with timer of 8051? Explain, in detail, mode-0 of timer of 8051 microcontroller. **[06]**

OR

Q- 6 [b] What do you understand by BIT addressing? Explain the BIT addressing features of 8051 in detail. **[06]**
