[82]

SARDAR PATEL UNIVERSITY
M.Sc. (Electronics) I Semester Examination
Monday, 25ᵗʰ March, 2019 Time 10.00 am to 01.00 pm
PS01CELE23 - Microprocessor and Microcontroller Systems
Total Marks – 70

1. Figure to the right indicate maximum marks for the question

Q-1   **[08]**

A) If a 8-bit buffer IC is to be interfaced with 8085 processor in peripheral I/O mode, which control signal is used to move the data?

   i. $\overline{MEMW}$ ii. $\overline{MEMR}$

   iii. $\overline{IOR}$ iv. $\overline{IOW}$

B) To differentiate Memory Mapped I/O and I/O Mapped I/O, which control pin of 8085 is used?

   i. RD ii. ALE

   iii. $IO/\overline{M}$ iv. None of the above

C) To interface 4 K of ROM memory, how many number of address lines are required?

   i. 13   ii. 14

   iii. 15   iv. 12

D) The control word value to configure 8155 for following is : Port A as output, Port B as input and Port C as output.

   i. 03h   ii. 0Dh

   iii. 00h   iv. 0Bh

E) 8155 IC has total _____ locations of RAM on it

   i. 128   ii. 256

   iii. 2 K   iv. none of the above

F) In 8255 PPI, Mode -0 is possible for followings:

   i. Port A only   ii. Port B only

   iii. Port A and B only   iv. Port A, B and C

G) The size of stack pointer of 8051 is _____.

   i. 12 bits   ii. 14 Bits

   iii. 16 bits   iv. 1 Byte

H) For de-multiplexing address and data bus in 8085 interfacing, which control signal is used?

   i. IO/M ii. ALE

   iii. $\overline{RD}$ iv. WR

Q-2   Answer any seven, In short.(Two marks each)   **[14]**

1   Describe the role of IO/$\overline{M}$ line of 8085 processor in interfacing.

2   What is the difference between the Microprocessors and Microcontrollers?

3   With necessary timing diagram, explain the Handshake data input process.

4   What do you mean by edge sensitive pin and level sensitive pin?

(P.T.O.)

5 Differentiate between active low and active high signal?
6 Draw a circuit to generate the various control signals for I/O operation of 8085.
7 Name the five interrupt sources of 8051.
8 Describe, in brief, bit addressable memory location in 8051 microcontroller.
9 Why data bus of 8085 processor is bidirectional?

Q-3 [a] For following instructions, draw and explain the instruction execution timing [06] diagram in detail:

Address	Instruction
CA00H	OUT
CA01H	FFH

Q-3 [b] Design the interface to the RAM of 8155. The RAM address should start at [06] address AF00H. Give the range of memory.

OR

Q-3 [b] Design a circuit, with necessary control signals and chip select logic, to [06] interface the memory(EPROM) of 8755 chip for the address-range F000h to F7FFh.

Q-4 [a] Design an address decoder circuit for absolute address **A0h** to a peripheral [06] device. Use 3:8 Decoder IC for decoding the address.

Q-4 [b] Write the control word format of 8255. Explain it in detail. [06]

OR

Q-4 [b] Write a program segment to get a data byte from port A of 8155 and add 20h [06] to this data. Output the results to port C. Assume that 8155 is configured in peripheral I/O. Make necessary assumptions.

Q-5 [a] The following memory devices are to be interfaced to 8085. [06]
(i) 2K ROM (ii) 4K RAM. The EPROM address should start from location address 0000h & RAM at the location C000H. Draw the complete interface diagram

Q-5 [b] Show the format of PSW of 8051. Discuss, each bit of PSW in detail. [06]

OR

Q-5 [b] Draw the Jump instruction ranges of 8051 microcontroller. Also discuss the [06] various instructions available for jump and call operations.

Q-6 [a] Explain the internal RAM organization of 8051. Discuss how the switching [06] between register banks is possible. Give a sequence of instructions to switch from BANK-2 to BANK-3 of 8051.

Q-6 [b] List and explain two SFR's used to manage the timer section of 8051. [06]

OR

Q-6 [b] Explain briefly, the five different addressing modes of 8051 with suitable [06] instructions.

———X———