SARDAR PATEL UNIVERSITY<br>M.C.A.(First Semester) Examination<br>PS01CMCA02 Logical Organization of Computers<br>Monday, $6^{\text {th }}$ January, 2014

Time : 10:30 a.m. to 1:30 p.m.
Total Marks : 70
Note: Answers to the two sections must be written in separate answer-books.

## SECTION - I

1.(A) Specify the IEEE single-precision floating-point representations for the decimal 5
numbers 426.125 and -17.5 . Represent the final answer in hexadecimal.
(B) Describe the architecture and working of a pipeline machine with diagram. 5
2.(A) Answer the following questions in brief (ANY FIVE) :
(i) Which steps are involved in instruction execution by a CPU ?
(ii) Draw the diagram showing logical position of a cache memory. What is the locality principle?
(iii) Construct a Hamming code for the ASCII character ' B ' considering odd parity.
(iv) What is the octal equivalent of the hexadecimal number 58DA.24E? What is its binary equivalent?
(v) Distinguish between the direct and indirect addressing techniques. What are the drawbacks of immediate addressing technique?
(vi) What do you understand by a trap? List any four common conditions that can cause traps.
3. Explain ANY THREE from the following : 15
(i) Hard disks,
(ii) CD-ROM,
(iii) Design criteria for instruction formats,
(iv) Laser printer.

## SECTION - II

4.(A) Explain the 2 's complement adder-subtractor with a circuit diagram. 5
(B) State and prove the DeMorgan's theorems. 5
(C) Explain the logic circuit for the odd parity generator. 5
5.(A) Explain the 1 -of-10 decoder circuit diagram. 5
(B) What is a multiplexer? Explain the 16-to-1 multiplexer with circuit diagram. 5 Why is it called a data selector?
6. (A) What is a flip flop ? Draw the logic circuit of a clocked D latch.

Explain its truth table and timing diagram. Differentiate between level clocking and edge triggering.
(B) Explain ANY ONE from the following :
(i) Controlled Buffer Register, (ii) Ring counter.

