		SEAT No No. of Printed Pages	s:3
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		SARDAR PATEL UNIVERSITY	
		B. Sc (4 <sup>th</sup> Semester) US04CELE-02	
		Instrumentation and Digital Electronics	
		·	7/4/2019
		10:00 am to	
	12.		70 marks
Q.1 M	lultiple	le Choice Questions:	10
- <b>-</b>			10
1.	One c	can construct Binary to Gray convertor using	
	a)	AND gate	
	<b>b)</b>	OR gate	
	c)	XOR gate	
	d)	NAND gate	
2.	If pro	ropagation delay is low	
	a)	The circuit is faster	
	b)	The circuit is slow	
	c)	The circuit is with medium speed	
	d)	None of above	
3	If all th	the components of Astable multivibrator are matched it will generate	
٥.	a)	Spikes	
	b)	Ractangular wave	
	c)	Square wave	
	d)	Triangular wave	
Л	BC YIE	ifferentiation circuit is used to generate from clock pulses	
7,	a)	ifferentiation circuit is used to generate from clock pulses  Spikes	
	b)	Ractangular wave	
	c)	Square wave	
	d)	Triangular wave	
	uγ	THATIBUILD WAVE	

5. Astable mutivibrator has

One stable state

Two stable state

No stable state
Three stable state

a)

b)

c)

d)

ο.	A COL	inter is a circuit that counts	
	a)	Number of clock pulses that hit the Counter	
	b)	Time period of Clock Pulse	
	c)	One half the time period of clock pulse	
	d)	None of above	
7.	The t	otal number of natural counts through which a counter progresses is given	
		by where n is total number of FFs	
	a)	2 <sup>n</sup>	
	b)	2 <sup>n</sup> + 1	
	c)	2 <sup>n</sup> -1	
	d)	None of the above	
8.	Circu	it is very complex in case of	
	a)	Serial Counter	
	b)	Parallel Counter	
	ć)	Combinational Counter	
	d)	None of the above	
9.	Binar	y decade counter counts	
	(a)	10 states	
	(b)	2 states	
	(c)	20 states	
	(d)	5 states	
10.	BCD	2421 counter has	
	(a)		
	(b)	~	
	(c)	<del>-</del>	
	(a)	No illegal states	
Q. 2	Answ	rer any Ten questions in short.	20
	1. D	efine Noise immunity and Noise margin.	
	2. D	raw LSTTL NAND gate circuit.	
	3. D	efine Propagation delay.	
		/hat is advantage of D Flip Flop over RS Flip Flop.	
		/hat is RC differentiation?	

6. What is the advantage of combinational counter?

8. What is the advantage and disadvantage of serial counter?

7. Draw circuit of 4-bit serial counter.

	9. Draw combined circuit of Up/Down counter.	
	10. Draw decoding gate for states 2 and 8 of decade counter.	
	11. Draw circuit of shift counter using 3 FFs.	
	12. How many states are omitted in BCD 2421 counter? List them.	
Q.3	Explain any two applications of XOR gate.	10
	OR	
Q.3	Explain in detail working of TTL NAND gate with neat diagram and logic specifications.	10
Q. 4	Describe working of Edge triggered D Flip Flop.	10
	OR	
Q.4	Explain in detail working of Schmitt Trigger circuit.	10
Q.5	Explain working of Mod 8 Serial counter.	10
	OR	
Q.5	Explain Mod 8 Parallel counter.	10
Q.6	Explain working 3 stage shift counter.	10
0.6	OR SUB / DOWN	
Q.6 l	Explain working of UP/DOWN counter.	10