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SARDAR PATEL UNIVERSITY
B. Sc (4th Semester)
US04CELE-02
Instrumentation and Digital Electronics

12/4/16
10:30 to 1:30 pm
70 marks

Q.1 Multiple Choice Questions: 10

1. Pairity checker is used for checking
   (a) 1 bit error
   (b) 2 bit error
   (c) 3 bit error
   (d) 4 bit error
2. The full form of TTL
   (a) Transistor Transistor Logic
   (b) Terminal Transistor Logic
   (c) Transformer Transistor Logic
   (d) None of the above

3. The FAN-IN of a logic circuit is given by
   (a) Number of input that can be connected to a gate
   (b)Number of input that can be connected to a gate
   (c) Number of input that can be connected to a gate
   (d) None

4. _____ and _____ gates are used to construct comparator

   (a) AND and OR
   (b) NAND and XOR
   (c) XNOR and AND
   (d) NAND and NOR

5. In J K Flip Flop, J=K=1, then
   (a) Q=1
   (b) Q=forbidden state
   (c) Q=toggle
   (d) Last state

6. Toggle means

(a) SET
(b) Complement of previous state
(c) RESET
(d) Last state

7. Flip Flops can store ----------Numbers

(a) Binary
(b) Octal
(c) Hexadecimal
(d) Decimal

8. A counter is a circuit that counts
   (a) Number of clock pulses that hit the Counter
   (b) Time period of Clock Pulse
   (c) OFF time of clock Pulse
   (d) ON time of Clock Pulse

9. Delay time is more in case of
   (a) Serial Counter
   (b) Parallel Counter
   (c) Combinational Counter
   (d) None of the above

10. In order to construct down counter, FF needs to be triggered from

(a) True side of o/p of previous FF
(b) Flase side of o/p of previous FF
(c) Clock pulse
(d) None of the above

Q. 1 Answer any Ten questions in short. 20

1. Define FAN-IN of a logic circuit.
2. List all Logic specifications you know for a logic circuit.
3. Draw circuit of Half adder? What does it do?
4. What is advantage of D Flip Flop over RS Flip Flop.
5. Draw logic diagram of Comparator using XNOR gate?
6. What is the advantage of combinational counter?
7. State difference between serial and parallel counter?
8. Draw circuit of Mod-8 Serial Counter.
9. Draw waveform diagram for Mod-8 serial counter.
10. How many states are omitted in BCD 2421 counter. Name them.
11. Draw decoding gate for states 8 and 2 of decade counter.

12. Draw circuit of shift counter using 3 FFs.

Q.3 Describe any two applications of X-OR gate. 10

OR

Q.3 Explain in detail working of TTL NAND gate with neat diagram. 10

Q. 4 Describe working of Edge triggered D Flip Flop. 10

OR

Q.4 Explain in detail working of Schmitt Trigger circuit in detail. 10

Q.5 Explain working of Mod 8 ripple counter. 10

OR

Q.5 Explain Mod 6 Parallel counter. 10

Q.6 Explain 3 stage shift counter. 10

OR

Q.6 Explain working of Up/Down counter. 10

**********BEST OF LUCK **********