

[27]

Seat No : _____

No. of Printed Pages : 2

SARDAR PATEL UNIVERSITY

INFORMATION & TECHNOLOGY

T.Y.B.Sc.(Semester - V) Examination November – 2019

US05CINT06 : Computer Architecture and Microprocessor

Date: 22-11-2019, Friday

Time: 10-00 to 01-00 P.M.

Total Marks : 70

Q.1 Multiple choice questions:

[10]

1. The 14 – bit binary selection input and their combine value specified _____.
A. Control Word B. Common Word C. Cache Word D. Compact Word
2. The size of source input SEL A is _____ bits.
A. 1 B. 2 C. 3 D. 4
3. Stack use _____ list.
A. LIFO B. FIFO C. FILO D. LILO
4. The _____ contains an address to specify the desired location in memory.
A. Address Register B. Word Count Register
C. Control Register D. All of these
5. A special very high speed memory called a _____ is sometimes used to increase the speed of processing.
A. Main Memory B. Auxiliary Memory
C. Secondary Memory D. Cache
6. The performance of cache memory is frequently measured in terms of a quality called _____.
A. Hit B. Hit Ratio C. Miss D. None of these
7. Each manufacturer of a microprocessor has devised a symbolic code for each instruction is called _____.
A. ASCII Code B. BCD Code C. Mnemonic D. None of these
8. In a tightly coupled multiprocessor system, the destination is a _____.
A. Memory Modules B. Processor
C. Cross Points D. None of these
9. CRT Stands for _____.
A. Carbon Ray Tube B. Cathod Red Tube
C. Cathod Ray Tube D. None of these
10. The data bus is _____.
A. Bidirectional B. One Way C. Unidirectional D. None of these

- Q.2 Write answer in short (Any Ten) [20]
1. Define PUSH and POP operation of Stack.
 2. Define Prefix Notation with example.
 3. Define I/O Command.
 4. Define Bus Request (BR) and Bus Grant (BG).
 5. Define Virtual Memory.
 6. Define Cache memory.
 7. Define High Level Languages.
 8. Define Machine Level Languages.
 9. Define Microprocessor.
 10. Define Program Counter.
 11. Define Registers.
 12. Define Address Bus.

Q.3 (a) Explain RAM and ROM Chip in detail. [5]

Q.3 (b) Explain General Register Organization. [5]

OR

Q.3 (a) Explain Components of CPU. [5]

Q.3 (b) Explain Zero Address Instruction with example. [5]

Q.4 (a) Explain Binary Multiplication using Register Method. [4]

Q.4 (b) What is DMA? Explain DMA Controller. [6]

OR

Q.4 (a) Explain Main Memory in detail. [4]

Q.4 (b) What is DMA? Explain DMA Transfer. [6]

Q.5 (a) Explain Operating System. [5]

Q.5 (b) Explain 8085 Assembly Languages. [5]

OR

Q.5 (a) Explain Characteristics of Multiprocessor. [5]

Q.5 (b) Explain Time Sharing Common Bus structure. [5]

Q.6 Explain Multiprocessor Initiated Operation. Also Explain Internal Data Operation. [10]

OR

Q.6 Explain Memory Classification in detail. Also explain Memory and Instruction Fetch. [10]

—X—
②