SEAT No. _____ No. of Printed Pages : 2

SARDAR PATELL UNIVERSITY

Fifth (Vth) Semester (CBCS) B. Sc. Examination

[113]

Tuesday, 29th December 2020

Time : 02:00 P.M. to 04:00 P.M.

Subject : PHYSICS [US05CPHY24]

ANALOG AND DIGITAL CIRCUITS

Total Marks : 70

Note : All the symbols have their usual meaning.

Q.1 **Write correct answer for each of the following MCQs. (Attempt All)** **(10)**

1. In low frequency response of a CE amplifier the ratio $\left|\frac{A_{v\,(LF)}}{A_{v\,(MF)}}\right| =$ _____.

   (a) 0 (b) $1/2$ (c) $1/\sqrt{2}$ (d) $1/\sqrt{3}$

2. The frequency at which CE short circuit high frequency current gain drops to unity is denoted by _____.

   (a) f_α (b) f_β (c) f_{hfb} (d) f_T

3. The optimum conversion efficiency of class B push-pull amplifier is _____.

   (a) 25% (b) 78.5% (c) 50% (d) 75.8%

4. An ideal Operational Amplifier has _____

   (a) infinite bandwidth (b) infinite output impedance

   (c) zero input impedance (d) none of the above

5. The feedback resistor is replaced by _____ when OP-AMP is used as an Integrator.

   (a) diode (b) Transistor (c) short circuit (d) capacitor

6. The ASCII code is a _____ bit code.

   (a) 8 (b) 7 (c) 16 (d) 32

7. A standard TTL gate has a power dissipation of _____ and propagation delay time of _____.

   (a) 22 mW, 6 ns (b) 1 mW, 35 ns (c) 10 mW, 10 ns (d) 20 mW, 3ns

8. The XOR logic gate output is high if the inputs are _____.

   (a) different (b) same (c) finite (d) infinite

9. A flip flop is _____ state device.

   (a) 2 (b) 4 (c) 8 (d) 16

10. In a positive edge triggered JK flip flop, a high J and a high K produce the _____ state.

    (a) low (b) high (c) toggle (d) inactive

Q.2 **Fill in the blanks and True-False. (Attempt All)** **(08)**

Fill in the blanks.

1. The maximum voltage gain in a CE amplifier is produced in _____ region.
2. The ratio of Differential Mode open loop gain to the Common Mode open loop gain is called _____.
3. De Morgan's first theorem says that a NOR gate is equivalent to bubbled _____ gate.
4. Small Scale Integration(SSI) refers to ICs with fewer than _____ gates on the chip.

State whether True or False

1. Class B push-pull amplifier is usually zero-biased.
2. If the two inputs to a differential amplifier are exactly the same, then the output is the signal multiplied by two.
3. Most TTL gates use the totem-pole output arrangement.
4. Shift registers are used to store and transfer data.

Q.3 **Answer briefly any ten of the following questions.** **(20)**

1. What are the functions of emitter bypass capacitor and coupling capacitor in transistor amplifier?
2. Explain : Crossover distortion.
3. Explain the drawbacks of transistor phase inverter circuit.
4. Explain Operational Amplifier.
5. List out the ideal characteristics of Op Amp.
6. Briefly explain unity gain bandwidth and slew rate.
7. Convert following hexadecimal numbers to binary numbers.
   (i) C5E2 (ii) CD42
8. Explain briefly : ASCII code.
9. Compare IC 7400 and IC 5400 series TTL gates.
10. Explain race condition.
11. What are functions of PRESET and CLEAR in flip-flop?
12. Define : Ring counter and Ripple counter.

Que.-4 **Answer any four of the following questions in detail** **[32]**

1. Discuss the high frequency model for CE amplifier. Explain base-spreading resistance and transistor transconductance.
2. Giving construction and working of class A push-pull amplifier, obtain the expression for the output current.
3. Draw the neat-labelled diagram and explain D.C. analysis of the bipolar differential amplifier having dual input balanced output configuration.
4. State the characteristics of ideal Op-Amp. Describe the application of Op-Amp, Summing Amplifier using inverting mode.
5. Giving proper logic circuit diagrams and truth tables explain Exclusive-OR gate and Exclusive-NOR gate.
6. Giving proper circuit diagram explain the working of two inputs TTL NAND gate. How better switching speed can be obtained with Schottky TTL?
7. Explain edge triggered D flip-flop giving suitable circuit diagram and truth table. Also compare edge triggering with level clocking.
8. Define Register. Explain the working of 4-bits Shift left and Shift right registers.

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