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		SARDAR PATEL UNIVERSITY	
	. 100	SARDAR PATEL UNIVERSITY  Fifth Semester B. Sc. Examination	
		Wednesday, 30 <sup>th</sup> December-2020	
		Time: 02:00 pm To 04:00 pm	
		Subject: PHYSICS [ <b>US05CPHY05</b> ]	
•		Analog Devices and Circuits	J 70
Nistes All i		Total Mar	KS: 7U
	-	nbols have their usual meanings.  nswer the MCQs choose the correct option.	[10]
Q-1	(1)	A JFET	[_0]
	(1)	(a) is a current control device (b) is a voltage control device	
		(c) has a low input resistance (d) has a very large voltage gain	
	(2)	The inversion layer is created in device.	
		(a) D-MOSFET (b) E-MOSFET	
		(c) N type JFET (d) P type JFET	
	(3)	The voltage that turns on an EMOS device is the	
		(a) pinchoff voltage (b) threshold voltage	
		(c) knee voltage (d) gate source cutoff voltage	
	(4)	In a small signal transistor amplifier voltage gain decreases in the higher	
		frequency range due to	
		(a) reactance of coupling capacitor (b) emitter resistor	
		(c) reactance of bypass capacitor (d) reactance of interelectrode capacitors	
	(5)	If base spreading resistance $r_{bb'} = 200$ ohm and $r_{b'e} = 800$ ohm then	
		h <sub>ie</sub> =ohm.	
		(a) 1000 (b) 700 (c) 850 (d) 150	
	(6)	The maximum achievable efficiency of a class A transformer coupled resistive	
•		load amplifier is	
	/****\	(a) 72.5% (b) 78.5% (c) 50% (d) 60%. In the class B condition of the power amplifier the output current flows	
	(7)	for	
		(a) less than half cycle of the input signal (b) half cycle of the input signal	
		(c) one and half cycle of the input signal (d) full cycle of the input signal	
	(8)	The operational amplifier (opamp) is a high gain coupled amplifier.	•
	(-)	(a) inductor (b) transformer (c) capacitor (d) direct	
	(9)	In an inverting opamp, input resistor $R_i$ is $1 \text{K}\Omega$ and feedback resistor $R_f$ is $10 \text{K}\Omega$ .	
		Its magnitude of closed loop voltage gain is	
		(a) 1000 (b) 100 (c) 10 (d)1	
	(10)	To use the inverting opamp as a logarithmic amplifier feedback resistor is	
		replaced by	
		(a) capacitor (b) diode (c) short circuit (d) transistor	[CO3
Que2	Do a	as directed.	[80]

- Mention whether the following statements are True or False. (A)
- N-channel JFET has pinch-off voltage  $V_p\!=6V$ . Its gate source cutoff voltage (1) V<sub>GS(off)</sub> will be -6V.
- For a CE transistor amplifier gain bandwidth product is given by  $f_T = h_{fe} f_{\beta}$ (2)

	(3)	To operate the transistor power amplifier in class A condition the operating point is set at cutoff.	
	(4)	To use the non-inverting opamp as a voltage follower the feedback resistor is	
	(B)	replaced by capacitor.  Fill in the blanks.	
	(5)	The transconductance of JFET is the ratio of	
	(6)	f <sub>T</sub> is the frequency at which CE short circuit current gain of transistor amplifier	
	(0)	drops to	
	(7)	The Conversion efficiency of a power amplifier is the ratio of	
	(8)	The common mode rejection ratio is defined as	
Q-3	Ansv	ver briefly Any Ten of the following questions.	[20]
	(1)	Give the construction of n channel JFET.	
	(2)	A JFET has $V_{GS(OFF)} = -6 \text{ V}$ and $I_{DSS} = 8 \text{ mA}$ . What are the gate voltage and drain current at the half cutoff point?	
	(3)	Explain briefly working of JFET chopper.	
	(4)	What is the function of coupling capacitor in a transistor amplifier?	
	(5)	Define $\alpha$ cutoff and $\beta$ cutoff frequencies in transistor amplifier.	
	(6)	Give the hybrid π circuit diagram of transistor amplifier with shorted load.	
	(7)	Draw the circuit diagram of class B complimentary symmetry amplifier.	
	(8)	State the drawbacks of transistor phase inverter circuit.	
	(9)	What is cross over distortion in class B push pull amplifier?	
	(10)	What is the use of universal balancing technique in opamp?	
	(11)	Define (i) output offset voltage and (ii) input offset voltage of opamp	
	(12)	Define (i) input bias current and (ii) input offset current of opamp.	
Que4		Define (i) input bias current and (ii) input offset current of opamp.  wer the following questions in detail. (Attempt any Four)	[32]
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