SARDAR PATEL UNIVERSITY
BSc (V Sem.) Examination
Tuesday, 27th November 2012
2.30 - 5.30 pm
US05CELE02 - Electronics (Digital Systems)

Total Marks: 70

Note: Figures to the right indicate full marks.

Q.1   Multiple choice questions.   [10]
  (i)   Shift register has _____.
        (a) Eight states   (b) No specified sequence of states
        (c) Five states
  (ii) In controlled Buffer register_____ is the control input.
        (a) Serial Input   (b) CLR
        (c) LOAD
  (iii) _____ registers are used in applications where power consumption
        and space are more important than speed as in a pocket calculator.
        (a) Static shift register
        (b) Universal shift register
        (c) Dynamic MOS register
  (iv) In 4 bit bidirectional shift register _____ Flip-Flops are used.
        (a) 6   (b) 3
        (c) 4
  (v)   The method of speeding up the addition process is based on _____
        and _____ functions.
        (a) Cin and Cout   (b) CG and CP
        (c) Cino and Cinl
  (vi) In serial adder _____ is used to save carry.
        (a) Register   (b) Flip-Flop
        (c) Counter
  (vii) The interface between the Modem and DTE is specified by an _____.
        (a) EIA   (b) IEA
        (c) AEI
  (viii) The full form of DTE is _____.
        (a) Data Transmission Equipment   (b) Data Terminal Equipment
        (c) Data Transition Equipment
  (ix) Which handshake line is sent by listener to indicate readiness for next
        byte?
        (a) NDAC   (b) NRFD
        (c) DAV
  (x)   A serial adder is used to add _____.
        (a) Parallel binary number   (b) Serial binary number
        (c) Serial and Parallel binary number

Q.2 Answer **Any Ten** questions in brief. [20]
  (i) Give the comparison between shift register and counter.
  (ii) In how many ways the data can be transmitted in shift register? Which are they?
  (iii) Draw the logic diagram of Controlled Buffer Register.
  (iv) What is Universal shift register?
  (v) What is the full form of ANSI and IEEE?
  (vi) Where are dynamic MOS registers used?
  (vii) Why serial adders are slower than parallel adder?
  (viii) Draw the logic diagram of full adder that produces CG and CP functions.
  (ix) How does the look ahead carry adder speed up the addition process?
  (x) What is full duplex transmission?
  (xi) Draw the circuit diagram which shows the totem pole outputs wired together may cause the excessive current through Q_1 of device A and Q_2 of device B.
  (xii) Draw the logic diagram of CMOS to low power Schoottky TTL Fanout=10.

Q.3 Explain 4 bit serial in serial out shift register giving necessary diagram and waveforms. [10]

OR

Q.3 Explain parallel in serial out shift register and parallel in parallel out shift register. [10]

Q.4
  (a) Discuss in detail the Bidirectional shift register briefly. [05]
  (b) Write a note on PLA device. [05]

OR

Q.4
  (a) Explain the applications of shift registers. [05]
  (b) Draw the logic diagram of universal shift register. [05]

Q.5
  (a) Discuss in detail the Two's complement addition and subtraction using parallel adders. [06]
  (b) Discuss in detail the serial adder. [04]

OR

Q.5
  (a) Discuss in detail the Binary multiplier. [06]
  (b) Explain in brief the BCD adder. [04]

Q.6
  (a) Explain the CMOS to TTL interfaces. [05]
  (b) Explain the TTL to CMOS interfaces. [05]

OR

Q.6
  (a) Write a note on Modems. [06]
  (b) Explain the Schmitt trigger as an interface. [04]

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