SEAT No._____ **SARDAR PATEL UNIVERSITY** No. of Printed Pages :

[73] **Fifth (Vth) Semester (CBCS) B. Sc. Examination**

Friday, 13th April, 2018

Time: 05:00 P.M. To 05:00 P. M.

Subject: PHYSICS [**US05CPHY05**]

ANALOG DEVICES AND CIRCUITS

Total Marks: 70

Note: All the symbols have their usual meanings.

Q-1 To answer the MCQs choose the correct option. [10]

(1) A P-channel JFET _____.

(a) is a voltage control device (b) is a current control device

(c) has a low input resistance (d) has a very large voltage gain

(2) N-channel JFET has pinch-off voltage $V_p = 6V$. Its gate source cutoff voltage $V_{GS(off)}$ will be _____.

(a) 4V (b) -6V (c) 3V (d) -3V

(3) The voltage that turns on an EMOS device is the _____.

(a) threshold voltage (b) pinch off voltage

(c) knee voltage (d) gate source cutoff voltage

(4) In a small signal transistor amplifier voltage gain decreases in the lower frequency range due to_____.

(a) reactance of coupling capacitor

(b) reactances of coupling capacitor and bypass capacitor

(c) reactance of bypass capacitor

(d) reactance of interelectrode capacitors

(5) If base spreading resistance $r_{bb'}$ = 150 ohm and $r_{b'e}$ = 850 ohm then h_{ie} =_____ohm.

(a) 1000 (b) 700 (c) 850 (d) 150

(6) The maximum achievable efficiency of a class A transformer coupled resistive load amplifier is _____.

(a) 72.5% (b) 78.5% (c) 50% (d) 60%.

(7) In the class A condition of the power amplifier the output current flows for_____.

(a) less than half cycle of the input signal

(b) half cycle of the input signal

(c) one and half cycle of the input signal

(d) full cycle of the input signal

(8) In a certain operational amplifier (opamp), the output voltage rises 4 V in 6 μs, its slew rate will be _____.

(a) 1.5 μs/V (b) 90 V/μs (c) 0.67 V/μs (d) 1.5 V/μs

(9) In a non-inverting opamp input resistor R_i is 1KΩ and feedback resistor R_f is shorted. Its closed loop voltage gain is_____.

(a) 1000 (b) 100 (c) 101 (d) 1

(10) To use the inverting opamp as an integrator feedback resistor is replaced by_____.

(a) capacitor (b) short circuit (c) diode (d) transistor

C.P.T.O.

Q-2 **Answer briefly Any Ten of the following questions.** [20]

(1) Give the construction of n channel JFET.

(2) A JFET has $V_{GS(OFF)}$ = -4 V and I_{DSS} = 5 mA. What are the gate voltage and drain current at the half cutoff point?

(3) Explain briefly working of JFET multiplexer.

(4) What is the function of emitter bypass capacitor in a transistor amplifier?

(5) Define α cutoff and β cutoff frequencies in transistor amplifier.

(6) Give the classification of small signal transistor tuned amplifiers.

(7) Draw the circuit diagram of class A transformer coupled resistive load amplifier.

(8) What is the function of input transformer in push pull amplifier?

(9) What is cross over distortion in class B push pull amplifier?

(10) What is a differential amplifier? Which are the various types of differential amplifiers?

(11) Define (i) CMRR and (ii) input offset voltage

(12) Define (i) input bias current and (ii) input offset current of opamp.

Q-3 Explain drain curves and transconductance curves of n-channel JFET with necessary diagrams. [10]

OR

Q-3 Describe construction and working of Enhancement mode MOSFET with suitable diagrams. Also explain its drain curves. [10]

Q-4 (a) Describe the procedure to obtain h-parameters of a transistor using equivalent circuit. [06]

(b) Write a note on gain bandwidth product. [04]

OR

Q-4 (a) Obtain the condition for maximum power transfer in a single tuned inductively coupled amplifier. [06]

(b) With the help of hybrid equivalent circuit of transistor amplifier derive the following equations. [04]

$$(i)\quad A_i = -\frac{h_f}{1+h_o R_L} \qquad (ii)\ A_v = \frac{A_i R_L}{R_i}$$

Q-5 (a) Describe the working of class A push pull amplifier and show that its output is free from even harmonics. [06]

(b) Write a note on transistor phase inverter circuit. [04]

OR

Q-5 (a) With necessary diagram show that maximum achievable efficiency in class B condition of push pull amplifier is 78.5%. [06]

(b) With suitable circuit diagram explain the working of class B complimentary symmetry amplifier. [04]

Q-6 (a) Give the circuit diagram of dual input balanced output configuration of differential amplifier and discuss its D. C. analysis. [06]

(b) Explain the application of an opamp as a difference amplifier. [04]

OR

Q-6 (a) State the characteristics of an ideal opamp. Explain the concept of virtual ground in inverting mode of an ideal opamp and obtain the expressions for its voltage gain. [06]

(b) Explain the application of an opamp as a logarithmic amplifier. [04]

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