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SARDAR PATEL UNIVERSITY

Fifth Semester B. Sc. Examination

Subject: PHYSICS [US05CPHY24]

Analog and Digital Circuits

Date: 14/11/2022 (Monday)

Time:10:00 A.M. To 01:00 P.M. **Total Marks: 70**

Note:(i)All the symbols have their usual meanings.

(ii) Figures at the right side of questions indicate full marks.

Que.-1 **To answer the MCQs choose the correct option.** **[10]**

1. The maximum achievable efficiency of a class A transformer coupled resistive load amplifier is _____.
   (a) 72.5% (b) 78.5% (c) 50% (d) 60%.
2. In the class B condition of the power amplifier the output current flows for_____.
   (a) full cycle of the input signal
   (b) less than half cycle of the input signal
   (c) one and half cycle of the input signal
   (d) half cycle of the input signal
3. To use the operational amplifier (opamp) as an integrator the feedback resistor is replaced by ____.
   (a) capacitor (b) diode (c) short circuit (d) transistor.
4. The opamp is a high gain _____ coupled amplifier.
   (a) transformer (b) direct (c) capacitor (d) inductor
5. A byte is a string of ____bits.
   (a) 8 (b) 2 (c) 4 (d) 16
6. The universal gates are_____.
   (a) AND, OR & NOT (b) NAND & NOR
   (c) NAND, NOR, AND, OR & NOT (d) AND & OR
7. The input transistor of 7400 TTL logic family consists of _____ .
   (a) multiple emitter (b) multiple collector
   (c) multiple base (d) single emitter
8. A flip flop is used to store ____ bit of information.
   (a) 1 (b) 8 (c) 4 (d) 2
9. How many flip flops are required to load 1011 binary number into register?
   (a) 2 (b) 4 (c) 3 (d) 1
10. A three bit ripple counter has a modulus of ____.
    (a) 4 (b) 16 (c) 8 (d) 2

Que.-2 **Answer *briefly* any ten of the following questions.** **[20]**

(1) Define α cutoff and β cutoff frequencies in transistor amplifier.

(2) What is cross over distortion in class B push pull amplifier?

(3) State the draw-backs of phase inverter circuit.

(4) Define following opamp parameters;
(i) input offset voltage and (ii) output offset voltage

P.T.O.

(5) Define (i) CMRR and (ii) slew rate of opamp.

(6) When does the opamp work as a voltage follower?

(7) Convert the hexadecimal number 2C to its equivalent decimal number.

(8) Explain briefly about ASCII code.

(9) State de Morgan's theorems.

(10) Explain in brief D flip-flop.

(11) Explain in brief working of JK master slave flip flop.

(12) What is a register? What is the function of shift register?

Que.-3 **(a)** Explain the function of emitter bypass capacitor in a transistor amplifier and discuss its effect on low frequency response of a transistor amplifier with the help of equivalent circuit. **[06]**

(b) Write a note on gain bandwidth product of a transistor amplifier. **[04]**

OR

Que.-3 **(a)** Describe the working of class A push pull amplifier and show that its output is free from even harmonics. **[06]**

(b) With suitable circuit diagram explain the working of class B complimentary symmetry amplifier. **[04]**

Que.-4 **(a)** Give the circuit diagram of dual input balanced output configuration of differential amplifier and discuss its D. C. analysis. **[06]**

(b) Explain the universal balancing technique to balance offset voltages in an opamp. **[04]**

OR

Que.-4 **(a)** State the characteristics of an ideal opamp. Explain the concept of virtual ground in inverting mode of an ideal opamp and obtain the expressions for its voltage gain. **[06]**

(b) Explain the application of an opamp as a logarithmic amplifier. **[04]**

Que.-5 **(a)** Explain the working of the two inputs AND gate with suitable circuit diagram. Which gate is implemented when its output is inverted? **[06]**

(b) (i) Convert the following binary numbers to decimal numbers **[04]**
(1) 1110 (2) 1110111
(ii) Convert the following hexadecimal numbers to binary numbers
(1) 9AC (2) B5E2

OR

Que.-5 **(a)** Explain the working of two inputs TTL NAND gate with suitable circuit diagram. **[06]**

(b) Describe the working of a NOT gate with suitable circuit diagram. **[04]**

Que.-6 **(a)** With suitable logic diagram explain the working of clocked JK flip-flop. **[06]**

(b) Explain working of RS flip flop implemented with NOR gates. **[04]**

OR

Que.-6 **(a)** Describe the working of four bit ripple counter with suitable logic diagram and clocked waveform. **[06]**

(b) Explain the working of 4-bit ring counter with suitable logic diagram. **[04]**