SARDAR PATEL UNIVERSITY
Programme & Subject: M.Sc – Information Technology (Integrated)
Semester: V
Syllabus with Effect from: June - 2014

Paper Code: PS05CIIT02	**Total Credit: 3**
Title of Paper: Computer Architecture	

Unit	Description in Detail	Weightage (%)
I	**Basic Computer Organization** Instruction Code Computer Register Computer Instructions Timing and Control Instruction Cycle Register Reference Instructions Memory Reference Instructions Input – Output Interrupt **Types of Interrupt** External Interrupt Internal Interrupt Software Interrupt	25%
II	**Central Processing Unit** Introduction **General Register Organization** Control Word **Stack Organization** Register Stack Memory Stack **Reverse Polish Notation** **Instruction Formats** Zero Address Instructions One Address Instructions Two Address Instructions Three Address Instructions **Addressing Mode** **Data Transfer and Manipulation** Data Transfer Instruction Data Manipulation Instructions Arithmetic Instructions Logical and Bit Manipulation Instructions Shift Instructions **Program Control** Status Bit Condition Conditional Branch Instruction	25%
III	**Pipeline and Vector Processing** Parallel Processing Pipelining Arithmetic Pipeline **Instruction Pipeline** Four Segment Instruction Pipeline	25%

	Data Dependency Handling of Branch Instruction **Vector Processing** Vector Operations Matrix Multiplication Memory Interleaving Superscalar Processors Supercomputers **Array Processor** Attached Array Processor SIMD Array Processor	
IV	**Input-Output Organization** **Peripheral Devices** **Input – Output Interface** I/O Bus and Interface Modules I/O versus Memory Bus **Asynchronous Data Transfer** Strobe Control Handshaking **Asynchronous Serial Transfer** **Asynchronous Communication Interface** Mode of Transfer **Direct Memory Access (DMA)** DMA Controller DMA Transfer	25%

Basic Text & Reference Books:

- Computer System Architecture, Third Edition, By M. Morris Mano
- Computer Organization and Architecture, 4th Edition By William Stallings