SARDAR PATEL UNIVERSITY
Programme & Subject: B.Sc. (CA & IT) – M.Sc. (CA & IT) Dual Degree
Semester – II
Syllabus with Effect from: June-2016

Paper Code: PS02EIIT01		**Total Credit: 2**
Title Of Paper: Digital Electronics		
Unit	**Description in detail**	**Weightage (%)**
I	**Basic Digital Logic Circuit-I** De – Morgan's Theorems Half Adder Full Adder Binary Adder 2's Complements Adder – Subtracter Encoder(8 X 3 line) Decoder(3 X 8 line)	25%
II	**Basic Digital Logic Circuit-II** Seven Segment Decoder Multiplexer (4 X 1, 8 X 1, 16 X 1 line) Nibble Multiplexer De-Multiplexer (1 X 4, 1 X 8, 1 X 16 line) Comparator	25%
III	**KarnaughMap** Boolean Relations Sum of Product Method Karnaugh Map up to 4 variables Karnaugh Map Simplifications Don't Care Conditions	25%
IV	**Memory Elements & Counters** RS Flip-Flop D Flip-Flop JK Flip-Flop JK Master Slave Flip-Flop Shift – Left & Shift – Right Control Buffer Register Ring Counter	25%

Basic Text & Reference Books:-

Malvino A. P. : Digital Computer Electronics, 3rd Edition, Tata McGraw - Hill Pub. Co. Ltd. , New Delhi, 1990

Gothmann, William H. : Digital Electronics – An Introduction to Theory and Practice , 2nd Edition, PHI , 1982.

Tanenbaum A. S. : Structured Computer Organization, 3rd Edition, Prentice-Hall of India Pvt. Ltd., 1993.