SARDAR PATEL UNIVERSITY Programme: B.Sc (Information Technology) Semester: V Syllabus with effect from: June - 2013

Paper Code: US05CINT06	Total Credit: 3
Title of Paper: Computer Architecture & Software Engineering	Total Credit: 5

Unit	Description in detail	Weightage (%)
I	Central Processing Unit & Input – Output Organization	weightage (70)
	Introduction	
	General Register Organization	
	Stack Organization	
	Register Stack	
	Memory Stack	
	Reverse Polish Notation	
	Instruction Formats	0504
	Zero-Address Instructions	25%
	One-Address Instructions	
	Two-Address Instructions	
	Three-Address Instructions	
	Peripheral Device	
	Input – Output Interface	
	I/O Bus and Interface Modules	
	I/O versus Memory Bus	
II	Computer Arithmetic & Memory Organization	
	Direct Memory Access	
	DMA Controller	
	DMA Transfer	
	Multiplication & Division using Register Methods	
	Memory Hierarchy	
	Memory Unit	25%
	Random-Access Memory	
	Read Only Memory	
	Virtual Memory	
	Address Space and Memory Space	
	Cache Memory	
	Associative Mapping	
III	Multiprocessor, Microprocessors & Microcomputers	
	Characteristics of Multiprocessor	
	Interconnection Structure	
	Time – Shared Common Bus	
	Multiport Memory	
	Crossbar Switch	
	Multistage Switching Network	25%
	Microprocessor	
	Microprocessor Instruction Set	
	Machine Language	
	8085 Machine Language	
	8085 Assembly Language	
	High Level Language	



	Operating System	
IV	Microprocessor Architecture and Microcomputer systems	
	Microprocessor Architecture and its operations	
	Microprocessor – initiated Operations and 8085 Bus organization	
	Internal Data Operations and 8085 Registers	25%
	Memory and Instruction Fetch	
	Memory Classification	
	Input / Output Devices	

Basic Text & Reference Books:

- Computer System Architecture by M. Morris Mano PHI Publication
 Microprocessor Architecture, Programming and Applications with the 8085 Third Edition by Ramesh S. Gaonkar Penram International

