SARDAR PATEL UNIVERSITY

Vallabh Vidyanagar

NAAC 'A' Grade (10-01-2023 To 09-01-2028)

NEP-2020 aligned Curriculum with effect from Academic Year 2026-27

P.G. Diploma in Semiconductor Science and Technology Semester-I

Course Type	Course Code	Course Title	Teaching-Learning Scheme	Total Notional Hours	Course credits
			L-P-T		
DSC	PGD01CSST01	Semiconductor Ecosystem, Devices and Technology	4-0-0	120	04

- **Course Learning Outcomes (CLOs)**

On completion of this course, students will be able to:

CLO1: Examine the global and national semiconductor ecosystem, detailing clean room infrastructure, supply chain dynamics and chip fabrication process flows.

CLO2: Analyze the physical properties and biasing conditions of intrinsic and extrinsic semiconductors, specifically evaluating the I-V characteristics and operational limitations of P-N junction diodes.

CLO3: Evaluate the structural design, performance metrics, and operating principles of semiconductor optoelectronic devices, including solar cells, LEDs, photodetectors and lasers.

CLO4: Investigate the electrical characteristics of metal-semiconductor contacts and heterojunctions.

CLO5: Analyze energy-band diagrams, equilibrium electrostatics, and interconnect parameters to determine their impact on charge transport and overall device behavior.

Unit	Course Content	Learning Pedagogies*	CLO(s)
I	**The Historical progress and Semiconductor Ecosystem in India** Scientific Progress from Ancient to modern Era, Growth and Evolution of the Indian Semiconductor Sector, Global Semiconductor Market Overview, Semiconductor Manufacturing Chain: Front-End and Back-End Processes, Industry Segments: Chip IP Cores, Electronic Design Automation (EDA) Tools, Specialized Materials and Chemicals, Wafer Fab Equipment (WFE), Fabless Companies, Integrated Device Manufacturers (IDMs) and Foundries, OSAT/ATMP, Cleanroom Facilities and Semiconductor Fabrication Environment, Semiconductor Chip Production Sequence, Semiconductor Supply Network and Market Dynamics in National and International Context, Government Policies and Strategic Programs including India Semiconductor Mission (ISM) and Production Linked Incentive (PLI) Scheme for Semiconductor Manufacturing.	CL, SDL, Visit	CLO1
II	**Fundamentals and Applications of Semiconductor Diode** Electrical Energy Generation and Storage Concepts in Ancient Indian Literature, Bonds in Semiconductors, Widely used Semiconductors: Si and Ge, Superiority of Silicon over	CL, PBL, IBL	CLO2

	Germanium, Temperature influence on Semiconductors, Intrinsic and Extrinsic Semiconductor, P-N Junction's Properties and Biasing, I-V Characteristics of P-N Junction, Diode as switch, Important Terms: Breakdown Voltage and Knee Voltage, Limitations in the Operating Condition of PN Junction: Maximum Forward Current, Peak Inverse Voltage (PIV) and Maximum Power Rating, Comparison of rectifier circuits, P-N Junction Application: Clipper and Clamper Circuit, Zener Diode, Diodes used in Microwave and RF Operation.		
III	**Optoelectronics in Semiconductor** Light properties explained by Sanskrit Slokas, Optical Absorption in Semiconductors, Determination of Optical Bandgap via UV-VIS-NIR spectroscopy, Photocurrent in a P-N Diode, Solar Photovoltaic Cell Construction and Current–Voltage Characteristics, Limiting Factors of Solar Cell Efficiency (Shockley-Queisser Limit), Photoconductive Detector, P-I-N Photodetector, Avalanche Photodiode, APD Design Issues, Light Emitting Diodes (LEDs): Operating Principle, Device Structure, Materials used for LED, LED Performance Issues, Advanced LED Structures, Semiconductor Lasers: Spontaneous and Stimulated Emission mechanism, Optical Cavity, Optical Absorption, Loss and Gain in Laser System, Role of Optoelectronic Sensors in AI hardware.	CL, SM, ICT	CLO3
IV	**Metal-Semiconductor junctions and Semiconductor Heterojunctions** Metal-Semiconductor Junction: Contacts Between Materials, Work Function and Electron Affinity, The Schottky Barrier Diode: Qualitative Characteristics, Ideal Junction behaviour, Nonideal Effects on the Barrier Height, I-V Relationship, Differentiation between Schottky Barrier Diode and the P-N Junction Diode, Metal-Semiconductor Ohmic Contacts: Ideal Nonrectifying Barriers, Tunneling Barrier, Specific Contact Resistance, Applications of Schottky diode. Semiconductor Heterojunctions: Materials and Energy band Diagrams, Two-Dimensional Electron Gas (2DEG), Equilibrium Electrostatics, Current-Voltage Characteristics, Metal Interconnect Parameters, Numerical Examples	CL, ICT, ROL, IBL	CLO4, CLO5

(*) Learning Pedagogies/Methods

(a) CL: Classroom Lecture
(b) SM: Seminars (Student-led and Faculty-moderated)
(c) CBL: Case-Based Learning
(d) MPR: Micro-Projects/Mini Research Tasks
(e) Visit: Industrial Visit/Field Visit/Institutional Visit
(f) PBL: Problem-Based Learning
(g) ROL: Research-Oriented Learning (Literature Review, Tool Construction, Data Analysis Exercises)

(h) COL: Collaborative Learning (Group Tasks, Peer Discussion, Joint Presentations)
(i) EL: Experiential Learning (Community Engagement, Internship-linked Activities, Practice-based Tasks)
(j) SRP: Simulation and Role-Play (Academic, Professional, or Policy-based Scenarios)
(k) ICT: ICT-Enabled Learning (LMS-based Tasks, Digital Resources, Virtual Labs/Webinars)
(l) RP: Reflective Practices (Learning Journals, Reflective Notes, Concept Mapping)
(m) IBL: Inquiry-Based Learning
(n) SDL: Self-Directed Learning (Guided Readings, Concept Exploration Tasks)

- **Assessment Methodologies**

(A) Internal Assessment [Total: 50 Marks]

a. Internal Formative assessment

(a) Assignment
(b) Seminars
(c) Class Regularity

b. Internal Summative Assessment

(a) Quizzes
(b) Mid-term tests

(B) Weightage of Learning Efforts for External Assessment [Total: 50 Marks]

Unit	Aligned CLOs	Total Learning Hours	Approximate weightage (Marks) to Learning levels (BT)			Total Marks
			Remember (R)	Understanding (U)	Application/ Analyse & above (A)	
I	**CLO1**	30	3	4	5	12
II	**CLO2**	30	2	5	5	12
III	**CLO3**	30	2	5	6	13
IV	**CLO4, CLO5**	30	2	6	5	13
		120	**09**	**20**	**21**	**50**

- **Assessment and Evaluation**

Sr. No.	Assessment/Evaluation	Component	Weightage (%)
1	Continuous Internal Evaluation	Mid-term tests, Seminars, Assignments, Quizzes, Class Regularity	50
2	End-Semester Examination	Written Exam Project Evaluation (Report, Presentation, Viva)	50

(C) CLOs – PLOs Matrix

CLO	PLO									
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10
CLO1	3	1	1	1	1	3	-	2	1	1
CLO2	3	1	3	1	3	1	2	1	1	1
CLO3	3	1	2	1	3	1	1	1	3	1
CLO4	2	3	3	3	2	1	1	1	1	3
CLO5	3	1	3	1	2	2	1	2	1	3

P.G. Diploma in Semiconductor Science and Technology Semester-I

Values to **CLO-PLO** matrix are assigned **by judging the importance of the particular CLO** in relation to the **PLOs**.

CLO – PLO correlation	Value
Strong	3
Moderate	2
Low	1
No correlation	-

- **Suggested Learning Materials Books:**

Sr. No.	Title	Author(s)	Edition/Year	Publisher
1	Principles of Electronics	V.K. Mehta & Rohit Mehta	12th Ed. (2020)	S. Chand Publishing
2	Semiconductor Devices: Physics and Technology	S.M. Sze & Kwok K. Ng	3rd Ed. (2012)	Wiley
3	Semiconductor Physics and Devices	Donald A. Neamen	4th Ed. (2021)	McGraw-Hill Education
4	Solid State Electronic Devices	Ben G. Streetman & Sanjay Banerjee	7th Ed. (2015)	Pearson
5	Modern Semiconductor Devices for Integrated Circuits	Chenming C. Hu	1st Ed. (2010)	Prentice Hall
6	Solid State and Semiconductor Physics	John P. McKelvey	Reprint (1982)	Krieger Pub. Co.
8	Metal-Semiconductor Contacts	William Rhoderick & Robert H. Williams	2nd Ed. (1988)	Oxford University Press
9	Semiconductor Devices: Basic Principles	Jasprit Singh	1st Ed. (2001)	John Wiley and Sons
10	Concise history of Science in India	D. M. Bose, S. N. Sen, B. V. Subbarayappa	2nd Ed. (2009)	Universities Press
11	Research Methodology for Natural Sciences	Prof. Soumitro Banerjee	2022	IISC Press

- **Online Resources (Open Source)**

Sr.No.	Description of Resource(s)	Weblink
1	A Google Sites page with resources on advanced semiconductor technology.	https://sites.google.com/view/advancedsemiconductors
2	An NPTEL course on semiconductor physics and devices by Prof. Digbijoy N. Nath, IISc.	https://archive.nptel.ac.in/courses/108/108/108108122/
3	An NPTEL course on PN Junction Diode	nptel.ac.in/courses/117107095
4	A presentation notes one LED	https://archive.nptel.ac.in/content/storage2/courses/117104022/Lectures/Lec15.pdf
5	An NPTEL course on Research Methodology for Natural Sciences	https://nptel.ac.in/courses/127106227

P.G. Diploma in Semiconductor Science and Technology Semester-I

Course Type	Course Code	Course Title	Teaching-Learning Scheme	Total Notional Hours	Course credits
			L-P-T		
DSC	PGD01CSST02	Fundamentals of Analog and Digital Circuits	4-0-0	120	04

- **Course Learning Outcomes (CLOs)**

On completion of this course, students will be able to:

CLO1: Analyze the fundamental characteristics and amplifier configurations of Bipolar Junction Transistors (BJTs).

CLO2: Design and evaluate analog and non-linear integrated circuits using Operational Amplifiers, Timer IC 555, and PLL IC 565 for applications signal conditioning, multivibrators, and voltage regulation.

CLO3: Apply number systems and fundamental logic functions to evaluate the transfer characteristics, current sourcing/sinking, and fan-out parameters of standard and specialized TTL gate families.

CLO4: Design combinational and sequential logic circuits and verify their performances.

CLO5: Classify the semiconductor memories and differentiates the microcontroller and micro processing systems.

Unit	Course Content	Learning Pedagogies*	CLO(s)
I	**Fundamentals of BJT** Introduction of BJT, Transistor Action, Transistor Connections: Common Base Connection, Characteristics of CB Transistor, Common Emitter Connection, Characteristics of CE Transistor, Simplified Transistor Current Relations, Common Collector Connection, Comparison of CB, CE and CC Transistor Action, Importance of CE Configuration, Transistor as an Amplifier in CE Arrangement, Transistor Load Line Analysis, Operating Point, Cut-off and Saturation Points, Numerical examples.	CL, ICT, SDL	CLO1
II	**Non-linear and Some Special Function Integrated Circuits** Operational Amplifier: Introduction, Internal Circuit of Operational Amplifier, Inverting and Non-Inverting Input and Polarity Relation, Bandwidth, Slew Rate, OP-Amp with Negative Feedback, Pin Diagram, Applications: Inverting Amplifier, Noninverting Amplifier, Voltage Follower, Multistage OP-Amp Circuits, Summing Amplifier, Integrator, Differentiator and Comparator circuits, Schmitt Trigger: UTP and LTP	CL, CBL, IBL	CLO2

	Adjustments, Digital to Analog and Analog to Digital Convertors using Op-Amp, Numerical Examples, Timer IC 555: Block diagram and pin description, Applications as Astable, Monostable, Bistable Multivibrator, PLL IC 565: Block diagram, pin description and Operation, Fixed voltage Regulator ICs 78xx and 79xx series, Introduction to SMPS.		
III	**Principles of Digital Systems and TTL Families** Invention of Zero by Aryabhatta, Coding in ancient India and Mahrishi Panini's contribution, Binary, Octal, Decimal, Hexadecimal Number Systems and their, Conversion, fundamentals of Analog and Digital Signals, Basic Logic Functions, IC-Gates related terminologies, RTL and DTL Gates, TTL Gates and Transfer Characteristics, Current Source and Sinking, Calculation of Fanout of Standard TTL Gates, Brief Introduction to TTL Families (74S, 74L, 74LS, 74ALS), Open Collector Gates and Buffer Drivers, Tri-State Logic Gate.	CL, SM, ROL	CLO3
IV	**Combinational, Sequential logic circuits and Memory** Moore's Law, Transition from Small Scale to Ultra Large-Scale Integration (SSI-ULSI), Outline of De Morgan's Theorems, Simplification of Boolean Expression and its related mathematics. Half - Full Adder and Subtractor, Concept of Flip-Flop and its various types including S-R, J-K, D and T Flip-Flop, Encoder and Decoders, Multiplexers and De-multiplexers, Registers, Counters, Classification of Semiconductor Memories, Introduction to Microprocessor, Microcontroller and Embedded System.	CL, MPR, ICT, EL	CLO4, CLO5

(*) Learning Pedagogies/Methods

(a) CL: Classroom Lecture
(b) SM: Seminars (Student-led and Faculty-moderated)
(c) CBL: Case-Based Learning
(d) MPR: Micro-Projects/Mini Research Tasks
(e) Visit: Industrial Visit/Field Visit/Institutional Visit
(f) PBL: Problem-Based Learning
(g) ROL: Research-Oriented Learning (Literature Review, Tool Construction, Data Analysis Exercises)
(h) COL: Collaborative Learning (Group Tasks, Peer Discussion, Joint Presentations)
(i) EL: Experiential Learning (Community Engagement, Internship-linked Activities, Practice-based Tasks)
(j) SRP: Simulation and Role-Play (Academic, Professional, or Policy-based Scenarios)
(k) ICT: ICT-Enabled Learning (LMS-based Tasks, Digital Resources, Virtual Labs/Webinars)
(l) RP: Reflective Practices (Learning Journals, Reflective Notes, Concept Mapping)
(m) IBL: Inquiry-Based Learning
(n) SDL: Self-Directed Learning (Guided Readings, Concept Exploration Tasks)

P.G. Diploma in Semiconductor Science and Technology Semester-I

- **Assessment Methodologies**

(A) Internal Assessment [Total: 50 Marks]

a. Internal Formative assessment

(a) Assignment
(b) Seminars
(c) Class Regularity

b. Internal Summative Assessment

(a) Quizzes
(b) Mid-term tests

(B) Weightage of Learning Efforts for External Assessment [Total: 50 Marks]

Unit	Aligned CLOs	Total Learning Hours	Approximate weightage (Marks) to Learning levels (BT)			Total Marks
			Remember (R)	Understanding (U)	Application/ Analyse & above (A)	
I	**CLO1**	30	3	4	5	12
II	**CLO2**	30	2	5	5	12
III	**CLO3**	30	2	5	6	13
IV	**CLO4, CLO5**	30	2	6	5	13
		120	**09**	**20**	**21**	**50**

- **Assessment and Evaluation**

Sr. No.	Assessment/Evaluation	Component	Weightage (%)
1	Continuous Internal Evaluation	Mid-term tests, Seminars, Assignments, Quizzes, Class Regularity	50
2	End-Semester Examination	Written Exam Project Evaluation (Report, Presentation, Viva)	50

(C) CLOs – PLOs Matrix

CLO	PLO									
	PLO1	**PLO2**	**PLO3**	**PLO4**	**PLO5**	**PLO6**	**PLO7**	**PLO8**	**PLO9**	**PLO10**
CLO1	3	1	2	1	2	1	2	1	1	1
CLO2	2	1	3	3	2	1	1	1	1	2
CLO3	2	1	3	1	2	1	3	-	1	1
CLO4	1	1	2	3	1	-	3	-	1	1
CLO5	3	1	2	1	2	1	2	1	1	1

P.G. Diploma in Semiconductor Science and Technology Semester-I

Values to **CLO-PLO** matrix are assigned **by judging the importance of the particular CLO** in relation to the **PLOs**.

CLO – PLO correlation	Value
Strong	3
Moderate	2
Low	1
No correlation	-

- **Suggested Learning Materials Books:**

Sr. No.	Title	Author(s)	Edition/Year	Publisher
1	Principles of Electronics	V. K. Mehta, Rohit Mehta	12th Ed. (2020)	S. Chand Publication
2	Semiconductor Physics and Devices: Basic Principles	Donald A. Neamen	3rd Ed. (2003)	Tata McGraw-Hill
3	Integrated Circuits	K. R. Botkar	5th Ed. (2010)	Khanna Publishers
4	Electronic Principles	Albert Malvino & David Bates	9th Ed. (2020)	McGraw-Hill Education
5	Electronic Devices	Thomas L. Floyd	10th Ed. (2017)	Pearson Education
6	Op-Amps and Linear Integrated Circuits	Ramakant A. Gayakwad	4th Ed. (2015)	Pearson Education
7	Digital Electronics	A. Anand Kumar	4th Ed. (2016)	PHI Learning Pvt. Ltd.
8	Digital Fundamentals	Thomas L. Floyd	11th Ed. (2014)	Pearson Education
9	Linear Integrated Circuits	D. Roy Choudhury, Shail B. Jain	5th Edition	New Age International
10	Op-Amps and Linear Integrated Circuits	Robert F. Coughlin, Frederick F. Driscoll	6th Edition	Pearson
11	Linear Integrated Circuits	S. Salivahanan, V. S. Kanchana Bhaskaran	3rd Edition	McGraw Hill Education
12	Op-Amp and Linear ICs	David A. Bell	3rd Edition	Oxford University Press
13	Electronic Devices and Components	J. Seymour	1989	Longman Sc & Tech
10	Concise history of Science in India	D. M. Bose, S. N. Sen, B. V. Subbarayappa	2nd Ed. (2009)	Universities Press

11	Research Methodology for Natural Sciences	Prof. Soumitro Banerjee	2022	IISC Press

- **Online Resources (Open Source)**

Sr. No.	Description of Resource(s)	Weblink
1	Practical guide to building logic gates using transistors.	https://www.101computing.net/creating-logic-gates-using-transistors/
2	Video tutorial on designing NAND, AND, OR, and NOR gates.	https://www.youtube.com/watch?v=OWlD7gL9gS0
3	NPTEL course on device physics and circuits by Prof. M. Gopal.	https://onlinecourses.nptel.ac.in/noc21_ee80/preview
4	NPTEL course on integrated circuits by Prof. Sudeb Dasgupta.	https://onlinecourses.nptel.ac.in/noc21_ee86/preview
5	NPTEL course on digital system design by Prof. Gautam Saha.	https://onlinecourses.nptel.ac.in/noc25_ee20/preview
6	NPTEL Course on Integrated Circuits and Applications	https://onlinecourses.nptel.ac.in/noc25_ee43/preview
5	An NPTEL course on Research Methodology for Natural Sciences	https://nptel.ac.in/courses/127106227

P.G. Diploma in Semiconductor Science and Technology Semester-I

Course Type	Course Code	Course Title	Teaching-Learning Scheme	Total Notional Hours	Course credits
			L-P-T		
DSC	PGD01CSST03	Verilog HDL for Digital Design and Synthesis	4-0-0	120	04

- **Course Learning Outcomes (CLOs)**

On completion of this course, students will be able to:

CLO1: Apply Verilog HDL constructs and standard design flow to develop and simulate basic digital circuits.

CLO2: Analyze and implement structural and gate-level designs using modules, ports and hierarchical connections.

CLO3: Design digital systems using behavioural modelling techniques with appropriate procedural constructs and control statements.

CLO4: Evaluate the impact of timing controls, delays and different modelling approaches on circuit performance and correctness.

CLO5: Develop synthesizable Verilog descriptions by applying advanced modelling concepts and established synthesis guidelines.

Unit	Course Content	Learning Pedagogies*	CLO(s)
I	**Fundamentals of Verilog HDL and Design Methodology** Evolution of Computer Aided Digital Design, Emergence of HDLs, Typical Design Flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs, Design Methodologies, 4-bit Ripple Carry Counter, Modules, Instances, Components of a Simulation, Example, Lexical Conventions, Data Types, System Tasks and Compiler Directives.	CL, ICT, SDL	CLO1
II	**Structural Modelling using Modules and Gate-Level Design** Modules, Ports, List of Ports, Port Declaration, Port Connection Rules, Connecting Ports to External Signals, Hierarchical Names, Gate Types, AND/OR Gates, BUF/NOT Gates, Gate-level Multiplexer, 4-Bit Full Adder, Gate Delays, Typical Delays, Continuous Assignments, Implicit Continuous Assignment, Regular Assignment Delay, Expressions, Operand and Operators.	CL, SM, COL, IBL	CLO2
III	**Behavioural Modelling Techniques** Structured Procedures, Procedural Assignments, Blocking and Nonblocking Statements, Timing Controls, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel Blocks, Tasks and Functions, Procedural Continuous Assignments, Overriding Parameters, Conditional Compilation and Execution, Useful System Tasks.	CL, EL, PBL, IBL, SDL	CLO3
IV	**Advanced Modelling and Synthesis Concepts** Types of Delays, Distributed Delay, Lumped Delay, Pin-to-Pin Delays, Path Delays, Timing Checks, Delay Back-Annotation, Switch-Level Modelling, MOS Switches, CMOS Switches, UDP	CL, SM, MPR, COL, EL	CLO4, CLO5

	Basics, Combinational UDPs, Sequential UDPs, PLI Basics, PLI Applications, PLI Routines, Synthesis Concepts, Synthesis Guidelines, Coding for Synthesis, Designing with FPGAs.		

(*) Learning Pedagogies/Methods

(a) CL: Classroom Lecture
(b) SM: Seminars (Student-led and Faculty-moderated)
(c) CBL: Case-Based Learning
(d) MPR: Micro-Projects/Mini Research Tasks
(e) Visit: Industrial Visit/Field Visit/Institutional Visit
(f) PBL: Problem-Based Learning
(g) ROL: Research-Oriented Learning (Literature Review, Tool Construction, Data Analysis Exercises)
(h) COL: Collaborative Learning (Group Tasks, Peer Discussion, Joint Presentations)
(i) EL: Experiential Learning (Community Engagement, Internship-linked Activities, Practice-based Tasks)
(j) SRP: Simulation and Role-Play (Academic, Professional, or Policy-based Scenarios)
(k) ICT: ICT-Enabled Learning (LMS-based Tasks, Digital Resources, Virtual Labs/Webinars)
(l) RP: Reflective Practices (Learning Journals, Reflective Notes, Concept Mapping)
(m) IBL: Inquiry-Based Learning
(n) SDL: Self-Directed Learning (Guided Readings, Concept Exploration Tasks)

- **Assessment Methodologies**

(A) Internal Assessment [Total: 50 Marks]

a. Internal Formative assessment

(a) Assignment
(b) Seminars
(c) Class Regularity

b. Internal Summative Assessment

(a) Quizzes
(b) Mid-term tests

(B) Weightage of Learning Efforts for External Assessment [Total: 50 Marks]

Unit	Aligned CLOs	Total Learning Hours	Approximate weightage (Marks) to Learning levels (BT)			Total Marks
			Remember (R)	Understanding (U)	Application/ Analyse & above (A)	
I	**CLO1**	30	2	5	6	13
II	**CLO2**	30	2	5	5	12
III	**CLO3, CLO4**	30	2	4	7	13
IV	**CLO5**	30	2	4	6	12
		120	**08**	**18**	**24**	**50**

P.G. Diploma in Semiconductor Science and Technology Semester-I

- **Assessment and Evaluation**

Sr. No.	Assessment/Evaluation	Component	Weightage (%)
1	Continuous Internal Evaluation	Mid-term tests, Seminars, Assignments, Quizzes, Class Regularity	50
2	End-Semester Examination	Written Exam	50

(C) CLOs – PLOs Matrix

CLO	PLO									
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10
CLO1	1	2	1	1	-	-	3	-	-	-
CLO2	2	2	2	1	1	-	3	-	-	1
CLO3	2	3	2	2	1	-	3	-	1	-
CLO4	1	2	3	1	2	-	2	-	-	1
CLO5	1	3	2	3	2	1	3	-	-	2

Values to **CLO-PLO** matrix are assigned **by judging the importance of the particular CLO** in relation to the **PLOs**.

CLO – PLO correlation	Value
Strong	3
Moderate	2
Low	1
No correlation	-

- **Suggested Learning Materials Books:**

Sr. No.	Title	Author(s)	Edition/Year	Publisher
1	Verilog HDL: A Guide to Digital Design and Synthesis	Samir Palnitkar	2nd Ed. (2003)	Prentice Hall
2	Design Through Verilog HDL	T. R. Padmanabhan, B. Bala Tripura Sundari	2009	Wiley
3	Digital Design Using Verilog HDL	Charles H. Roth Jr., Larry L. Kinney	2nd Ed. (2013)	Cengage Learning
4	Advanced Digital Design with the Verilog HDL	Michael D. Ciletti	2nd Ed. (2011)	Pearson
5	Fundamentals of Digital Logic with Verilog Design	Stephen Brown, Zvonko Vranesic	3rd Ed. (2009)	McGraw-Hill
6	A Verilog HDL Primer	J. Bhasker	3rd Ed. (2005)	BSP Books Pvt. Ltd.

P.G. Diploma in Semiconductor Science and Technology Semester-I

- **Online Resources (Open Source)**

Sr. No.	Description of Resource(s)	Weblink
1	A Google Sites page with resources on advanced semiconductor technology.	https://sites.google.com/view/advancedsemiconductors
2	NPTEL course on Digital System Design using Verilog by Prof. Indranil Sengupta, IIT Kharagpur.	https://nptel.ac.in/courses/106105165
3	Video lecture on digital design Verilog HDL concepts.	https://youtu.be/vHLBO05TeyU?si=bcem3Mu1cLCJVyvF
4	Digital Design with Verilog:	https://onlinecourses.nptel.ac.in/noc26_cs24/preview
5	EDA Playground – Online Verilog Simulator for practice and experimentation.	https://www.edaplayground.com/

P.G. Diploma in Semiconductor Science and Technology Semester-I

Course Type	Course Code	Course Title	Teaching-Learning Scheme	Total Notional Hours	Course credits
			L-P-T		
DSC	PGD01CSST04	Practical-1	0-8-0	120	04

- **Course Learning Outcomes (CLOs)**

On completion of this course, students will be able to:

CLO1: Design, simulate and evaluate analog and digital electronic circuits using EDA tools to investigate circuit performance and operational characteristics.

CLO2: Analyze UV-Vis spectroscopy data to determine optical constants of thin films and correlate material properties.

CLO3: Develop and implement combinational logic circuits including logic gates, multiplexers, demultiplexers, encoders and decoders using Verilog HDL for digital system design.

CLO4: Construct and verify sequential logic systems such as flip-flops, registers and counters using Verilog HDL for synchronous digital operations.

CLO5: Integrate simulation, HDL programming and verification methodologies to optimize digital circuit functionality and hardware-oriented problem solving.

Unit	Course Content	Learning Pedagogies/Methods	CLO(s)
1	Simulation of Analog Circuits	ROL, COL, EL	CLO1
2	Simulation of Digital Circuits	ROL, COL, EL	CLO1
3	Optical Constants Determination of Thin Films using UV-Vis Spectroscopy	SRP, ICT, SDL	CLO2
4	Implement and verify the functionality of different gates using Verilog	SRP, ICT, SDL	CLO2, CLO3
5	Design and Simulation of Flip-Flops, Registers and Counters using Verilog	ROL, COL, EL, IBL	CLO4
6	Design and Simulation of Encoders and Decoders using Verilog	PBL, COL, EL	CLO3
7	Design and Simulation of Multiplexers and Demultiplexers using Verilog	ROL, COL, EL, IBL	CLO3
8	Design 4-bit binary, BCD counters using Verilog	ROL, COL, EL, IBL	CLO5

(*) Learning Pedagogies/Methods

(a) CL: Classroom Lecture
(b) SM: Seminars (Student-led and Faculty-moderated)
(c) CBL: Case-Based Learning
(d) MPR: Micro-Projects/Mini Research Tasks
(e) Visit: Industrial Visit/Field Visit/Institutional Visit

(f) PBL: Problem-Based Learning
(g) ROL: Research-Oriented Learning (Literature Review, Tool Construction, Data Analysis Exercises)
(h) COL: Collaborative Learning (Group Tasks, Peer Discussion, Joint Presentations)
(i) EL: Experiential Learning (Community Engagement, Internship-linked Activities, Practice-based Tasks)
(j) SRP: Simulation and Role-Play (Academic, Professional, or Policy-based Scenarios)
(k) ICT: ICT-Enabled Learning (LMS-based Tasks, Digital Resources, Virtual Labs/Webinars)
(l) RP: Reflective Practices (Learning Journals, Reflective Notes, Concept Mapping)
(m) IBL: Inquiry-Based Learning
(n) SDL: Self-Directed Learning (Guided Readings, Concept Exploration Tasks)

- **Assessment Methodologies**

(A) Internal Assessment [Total: 50 Marks]

a. Internal Formative assessment

(a) Preparation of Journal
(b) Practical Viva
(c) Laboratory Regularity

b. Internal Summative Assessment

(a) Mid-term Practical Examination
(b) Laboratory Performance

(B) Weightage of Learning Efforts for External Assessment [Total: 50 Marks]

Unit	Aligned CLOs	Total Learning Hours	Approximate weightage (Marks) to Learning levels (BT)			Total Marks
			Remember (R)	Understanding (U)	Application/ Analyse & above (A)	
Practical	CLO1, CLO2, CLO3, CLO4, CLO5	120	10	20	20	50

- **Assessment and Evaluation**

Sr.No.	Assessment/Evaluation	Component	Weightage (%)
1	Continuous Internal Evaluation	Mid-Term Practical Exam, Lab Performance Record/Journal, Internal Practical Viva, Attendance	50
2	End-Semester Examination	End-Term Practical Exam with Viva.	50

(C) CLOs – PLOs Matrix

CLO	PLO									
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10
CLO1	2	3	2	1	2	-	1	-	-	-
CLO2	2	2	3	1	3	2	-	-	1	-
CLO3	1	3	2	3	2	-	3	-	-	-
CLO4	2	3	3	2	3	-	3	-	-	-
CLO5	1	3	2	3	2	-	3	-	-	-

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Values to **CLO-PLO** matrix are assigned **by judging the importance of the particular CLO** in relation to the **PLOs**.

CLO – PLO correlation	Value
Strong	3
Moderate	2
Low	1
No correlation	-

- **Suggested Learning Materials Books:**

Sr. No.	Title	Author(s)	Edition/Year	Publisher
1	Principles of Electronics	V.K. Mehta & Rohit Mehta	12th Ed. (2020)	S. Chand Publishing
2	Electronic Principles	Albert Malvino & David Bates	9th Ed. (2020)	McGraw-Hill Education
3	Digital Electronics	A. Anand Kumar	4th Ed. (2016)	PHI Learning Pvt. Ltd.
4	Digital Fundamentals	Thomas L. Floyd	11th Ed. (2014)	Pearson Education
5	Verilog HDL: A Guide to Digital Design and Synthesis	Samir Palnitkar	2nd Ed. (2003)	Prentice Hall
6	Design Through Verilog HDL	T. R. Padmanabhan, B. Bala Tripura Sundari	2009	Wiley

- **Online Resources (Open Source)**

Sr. No.	Description of Resource(s)	Weblink
1	A Google Sites page with resources on advanced semiconductor technology.	https://sites.google.com/view/advancedsemiconductors
2	Virtual Labs: Digital Electronics	http://vlabs.iitkgp.ernet.in/dec/
3	Home page for CircuitMaker software	https://circuitmaker.com/
4	NPTEL course on Digital System Design using Verilog by Prof. Indranil Sengupta, IIT Kharagpur.	https://nptel.ac.in/courses/106105165
5	Video lecture on digital design Verilog HDL concepts.	https://youtu.be/vHLBO05TeyU?si=bcem3Mu1cLCJVyvF
6	Practical guide to building logic gates using transistors.	https://www.101computing.net/creating-logic-gates-using-transistors/
7	Video tutorial on designing NAND, AND, OR, and NOR gates.	https://www.youtube.com/watch?v=OWlD7gL9gS0

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Course Type	Course Code	Course Title	Teaching-Learning Scheme	Total Notional Hours	Course credits
			L-P-T		
DSC	PGD01CSST05	Practical-2	0-8-0	120	04

- **Course Learning Outcomes (CLOs)**

On completion of this course, students will be able to:

CLO1: Design and evaluate basic logic gate circuits and Boolean operations for digital electronic applications.

CLO2: Analyze and simulate Schmitt Trigger circuits, voltage comparators and zero-crossing detectors for signal conditioning applications.

CLO3: Investigate and interpret MOSFET characteristics using experimental approach.

CLO4: Develop and optimize PID control system and transmission line.

CLO5: Analyze thermoelectric power and pulse photo response characteristics for semiconductor and optoelectronic applications.

Unit	Course Content	Learning Pedagogies*	CLO(s)
1	Basic Logic gates and Boolean Operations with Applications	ROL, COL, EL	CLO1
2	Schmitt Trigger Circuits (Inverting and Non-Inverting)	SRP, ICT, SDL	CLO2
3	Voltage Comparator and Zero-Crossing Detector	SRP, ICT, SDL	CLO2
4	MOSFET Characteristics	ROL, COL, EL, IBL	CLO3
5	PID control	PBL, COL, EL	CLO4
6	Transmission Line Characteristics	ROL, COL, EL, IBL	CLO4
7	Thermoelectric Power Measurement	SRP, ICT, SDL	CLO5
8	Pulse Photo Response	ROL, COL, EL, IBL	CLO5

(*) Learning Pedagogies/Methods

(a) CL: Classroom Lecture
(b) SM: Seminars (Student-led and Faculty-moderated)
(c) CBL: Case-Based Learning
(d) MPR: Micro-Projects/Mini Research Tasks
(e) Visit: Industrial Visit/Field Visit/Institutional Visit
(f) PBL: Problem-Based Learning
(g) ROL: Research-Oriented Learning (Literature Review, Tool Construction, Data Analysis Exercises)
(h) COL: Collaborative Learning (Group Tasks, Peer Discussion, Joint Presentations)
(i) EL: Experiential Learning (Community Engagement, Internship-linked Activities, Practice-based Tasks)
(j) SRP: Simulation and Role-Play (Academic, Professional, or Policy-based Scenarios)
(k) ICT: ICT-Enabled Learning (LMS-based Tasks, Digital Resources, Virtual Labs/Webinars)

(l) RP: Reflective Practices (Learning Journals, Reflective Notes, Concept Mapping)
(m) IBL: Inquiry-Based Learning
(n) SDL: Self-Directed Learning (Guided Readings, Concept Exploration Tasks)

- **Assessment Methodologies**

(A) Internal Assessment [Total: 50 Marks]

a. Internal Formative assessment

(a) Preparation of Journal
(b) Practical Viva
(c) Laboratory Regularity

b. Internal Summative Assessment

(a) Mid-term Practical Examination
(b) Laboratory Performance

(B) Weightage of Learning Efforts for External Assessment [Total: 50 Marks]

Unit	Aligned CLOs	Total Learning Hours	Approximate weightage (Marks) to Learning levels (BT)			Total Marks
			Remember (R)	Understanding (U)	Application/ Analyse & above (A)	
Practical	CLO1, CLO2, CLO3, CLO4, CLO5	120	10	20	20	50

- **Assessment and Evaluation**

Sr.No.	Assessment/Evaluation	Component	Weightage (%)
1	Continuous Internal Evaluation	Mid-Term Practical Exam, Lab Performance, Record/Journal, Internal Practical Viva, Attendance	50
2	End-Semester Examination	End-Term Practical Exam with Viva.	50

(C) CLOs – PLOs Matrix

CLO	PLO									
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10
CLO1	2	2	2	1	2	-	3	-	-	-
CLO2	2	3	3	2	3	-	1	-	-	-
CLO3	3	2	3	2	3	2	-	-	-	-
CLO4	2	3	3	3	2	-	1	-	-	-
CLO5	2	2	3	1	3	2	-	-	3	-

Values to **CLO-PLO** matrix are assigned **by judging the importance of the particular CLO** in relation to the **PLOs**.

CLO – PLO correlation	Value
Strong	3
Moderate	2
Low	1
No correlation	-

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- **Suggested Learning Materials Books:**

Sr. No.	Title	Author(s)	Edition/Year	Publisher
1	Electronic Principles	Albert Malvino & David Bates	9th Ed. (2020)	McGraw-Hill Education
2	Digital Electronics	A. Anand Kumar	4th Ed. (2016)	PHI Learning Pvt. Ltd.
3	Linear Integrated Circuits	D. Roy Choudhury, Shail B. Jain	5th Ed.	New Age International
4	Op-Amps and Linear Integrated Circuits	Robert F. Coughlin, Frederick F. Driscoll	6th Ed.	Pearson
5	Op-Amp and Linear ICs	David A. Bell	3rd Ed.	Oxford University Press
6	Microwave Engineering	David M. Pozar	4th Ed. (2011)	Wiley
7	Introduction to Solid State Physics	Charles Kittel	8th Ed. (2004)	Wiley

- **Online Resources (Open Source)**

Sr. No.	Description of Resource(s)	Weblink
1	A Google Sites page with resources on advanced semiconductor technology.	https://sites.google.com/view/advancedsemiconductors
2	NPTEL course on integrated circuits by Prof. Sudeb Dasgupta.	https://onlinecourses.nptel.ac.in/noc21_ee86/preview
3	Video tutorial on designing NAND, AND, OR, and NOR gates.	https://www.youtube.com/watch?v=OWlD7gL9gS0
4	Virtual Labs: Digital Electronics	http://vlabs.iitkgp.ernet.in/dec/
5	MOSFET Characteristics	https://nptel.ac.in/courses/108108111
6	Study material for Thermoelectric power	https://archive.nptel.ac.in/content/storage2/courses/112106139/pdf/2_2.pdf

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Course Type	Course Code	Course Title	Teaching-Learning Scheme	Total Notional Hours	Course credits
			L-P-T		
DSC	PGD01CSST06	Research Project	0-2-0	60	02

- **Course Learning Outcomes (CLOs)**

On completion of this course, students will be able to:

CLO1: Identify and formulate semiconductor and electronic design automation (EDA) related problems through systematic literature review and technical investigation.

CLO2: Apply EDA tools, simulation platforms and appropriate analytical methodologies to design, model and evaluate semiconductor devices and electronic circuits.

CLO3: Analyze simulation outputs, circuit responses and experimental data using scientific reasoning and computational techniques for performance optimization.

CLO4: Develop professional technical documentation and communicate project outcomes effectively through reports, design files, demonstrations and presentations.

CLO5: Demonstrate independent learning, innovation, teamwork and research-oriented problem-solving skills in semiconductor and EDA-based project development.

Unit	Course Content	Learning Pedagogies*	CLO(s)
I	Research Project	SM, ROL, IBL, SDL, PBL, COL, EL, ICT, RP	CLO1, CLO2, CLO3, CLO4, CLO5

(*) Learning Pedagogies/Methods

(a) CL: Classroom Lecture
(b) SM: Seminars (Student-led and Faculty-moderated)
(c) CBL: Case-Based Learning
(d) MPR: Micro-Projects/Mini Research Tasks
(e) Visit: Industrial Visit/Field Visit/Institutional Visit
(f) PBL: Problem-Based Learning
(g) ROL: Research-Oriented Learning (Literature Review, Tool Construction, Data Analysis Exercises)
(h) COL: Collaborative Learning (Group Tasks, Peer Discussion, Joint Presentations)
(i) EL: Experiential Learning (Community Engagement, Internship-linked Activities, Practice-based Tasks)
(j) SRP: Simulation and Role-Play (Academic, Professional, or Policy-based Scenarios)
(k) ICT: ICT-Enabled Learning (LMS-based Tasks, Digital Resources, Virtual Labs/Webinars)

(l) RP: Reflective Practices (Learning Journals, Reflective Notes, Concept Mapping)
(m) IBL: Inquiry-Based Learning
(n) SDL: Self-Directed Learning (Guided Readings, Concept Exploration Tasks)

. **Assessment Methodologies**

(A) Internal Assessment [Total: 25 Marks]

a. Internal Formative assessment

(a) Continuous Progress Monitoring
(b) Performance and Regularity

b. Internal Summative Assessment

(a) Internal Presentation
(b) Project Report

(B) Weightage of Learning Efforts for External Assessment [Total: 25 Marks]

Unit	Aligned CLOs	Total Learning Hours	Approximate weightage (Marks) to Learning levels (BT)			Total Marks
			Remember (R)	Understanding (U)	Application/ Analyse & above (A)	
I	CLO1, CLO2, CLO3, CLO4, CLO5	60	04	07	14	25

- **Assessment and Evaluation**

Sr.No.	Assessment/Evaluation	Component	Weightage(%)
1	Continuous Internal Evaluation	Continuous Progress Monitoring, Performance and Regularity, Internal Presentation, Project Report	50
2	End-Semester Examination	Project Evaluation: Final Report, Presentation and Viva Voce	50

(C) CLOs – PLOs Matrix

CLO	PLO									
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10
CLO1	2	2	2	1	2	-	1	-	-	-
CLO2	2	3	2	3	2	1	2	-	-	1
CLO3	2	3	3	2	3	-	2	-	1	-
CLO4	1	2	2	2	2	-	1	-	-	1
CLO5	2	2	3	2	2	1	2	-	1	-

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Values to **CLO-PLO** matrix are assigned **by judging the importance of the particular CLO** in relation to the **PLOs**.

CLO – PLO correlation	Value
Strong	3
Moderate	2
Low	1
No correlation	-

- **Suggested Learning Materials Books:**

Sr. No.	Title	Author(s)	Edition/Year	Publisher
1	Introduction to Semiconductor Manufacturing Technology	Stephen A. Campbell	2nd Ed. (2008)	McGraw-Hill Education
2	Research Methodology: Methods and Techniques	C.R. Kothari	2nd Ed. (2004)	New Age International
3	3D TCAD simulation for Semiconductor process, Devices and Optoelectronics	Simon Li and Yue Fu	2012	Springer New York, NY
4	SPICE for Circuits and Electronics Using PSpice	Muhammad H. Rashid	2nd Ed.	Cengage Learning
5	Research Methodology for Natural Sciences	Prof. Soumitro Banerjee	2022	IISC Press
6	The Electronic Design Automation Handbook	Dirk Jansen	1st Ed. (2003)	Springer New York, NY

- **Online Resources (Open Source)**

Sr. No.	Description of Resource(s)	Weblink
1	A Google Sites page with resources on advanced semiconductor technology	https://sites.google.com/view/advancedsemiconductors
2	Silvaco official webpage	https://silvaco.com/
3	NPTEL Course on Semiconductor device modeling and Simulation	https://nptel.ac.in/courses/108105188
4	NPTEL course on Semiconductor Physics and Devices by IISc	https://archive.nptel.ac.in/courses/108/108/108108122/